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A RECORDING SEISMIC SYSTEM FOR REFRACTION STUDIES AT SEA

by

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A RECORDING SEISMIC SYSTEM
FOR
REFRACTION STUDIES AT SEA

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ABSTRACT

A recording seismic system, designed primarily for use in refraction studies at sea, has been developed. It is completely self-contained and can be programmed to turn on and off at various pre-determined intervals. The recording section contains low frequency amplifiers, FM modulators, a digital clock and switching components. Four channels of information, including two levels of signal separated by 30 db, one timing channel and one reference frequency compensation channel, are recorded on a four track magnetic tape recorder. The playback system provides for reproducing records in the laboratory and a visual display of the time from the clock.

The system was successfully tested at sea on the Mid-Atlantic Ridge in July, 1968 and, at the time of writing this report, is being used in a seismic experiment being carried out by C.E. Keen in the same area.

ACKNOWLEDGEMENTS

The success of any graduate research project, such as this one, depends on the cooperation of a large number of people. I have been fortunate to be involved with a group of most encouraging and helpful colleagues, without whose interest and assistance this project would not have been possible.

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CHAPTER I

INTRODUCTION

This thesis describes a self-contained seismic recording system for use in areas where limits on available space and power make most conventional systems impractical. Although readily adapted for portable land use, the main application is in seismic refraction studies at sea.

An increasing interest in the ocean and the ensuing development of ocean technology over the last twenty years have made it possible to adopt many of the seismic techniques used on land for investigations at sea. The detailed structure of the oceanic crust and mantle is of great interest in the light of recent theories of ocean floor spreading, mid-ocean ridges, convection currents and transform faults. As a supplement to gravity and magnetic studies, explosion seismology offers one of the most useful methods in the attempt to determine the history and structure of the earth in oceanic areas.

Although much work has been done in developing recording systems for use on land and in shallow water, only a small number of specialized systems have emerged for use in deep sea areas.

The requirements of a system for use at sea are greatly different than those for land use. The elements of Nature limit the complexity of a system in many ways. Equipment must be sophisticated enough to obtain the data required but must be as simple as possible to be useful in a severe environment. Any components that do not remain on the ship during the recording operation must be small enough to allow for easy handling and yet sturdy enough to withstand rough treatment by man and the sea. They must be able to withstand the severity of moisture, acceleration and low temperature encountered on the sea. To be useful, they must be capable of unmanned operation for extended periods of time without constant surveillance.

Each problem to be investigated at sea has its unique requirements and a system designed with these in mind tends to be simpler and more economical than a general purpose instrument or one modified for the purpose. Thus, many instruments have been designed in accordance with the specialized problems of particular groups of scientists. The development of such an instrument is the subject of this work.

1.1 Seismic Recording at Sea

Methods of reflection seismic surveying at sea involving shipboard instrumentation and towed sensors are of little interest here. The interest is in refraction methods where the techniques involved (Shor, 1963) make it necessary to have sensors spaced at greater distances and larger spacing between energy source and receivers.

The first attempts at refraction lines in the deep sea were made by Ewing and Vine (1938) using geophones and explosive sources placed on the sea bed in 2000 meters of water and connected to the surface by a steel cable. Success was limited by cable noise and in 1940 they constructed a more successful free falling system equipped with a ballast release to return it to the surface (Ewing et al, 1946). Bullard and Gaskell (1941) suggested that hydrophones be used as receivers instead of geophones, thus removing the necessity of lowering instruments to the ocean floor. After World War II this practice was adopted (Hill and Willmore, 1947) and development continued along two lines, the Americans using a two ship system (Officer, Ewing, and Wuenschell, 1952) and the British a single ship and telemetering buoys (Hill, 1952, 1963).

The two ship system has proved successful but has a number of disadvantages. The added cost of operating two ships is obvious and, as well, the number and spacing of receivers is limited by the length of hydrophone array that can be towed. The sonobuoy system has the advantage of making it possible to use large array receiving techniques such as will be used by C. Keen on the Mid Atlantic Ridge during the summer of 1968.

The systems requiring only one ship fall into three categories:

1) Telemetering buoys operate from the sea surface, receiving seismic signals on crystal or ceramic hydrophones and telemetering information via a radio link back to the recording ship.

2) Recording buoys are similar to telemetering buoys but record information within the buoy itself on either photographic paper or magnetic tape.

3) Ocean bottom recorders are dropped from a ship to the ocean bottom, where they can receive information from both velocity sensitive geophones and pressure sensitive hydrophones. Information is recorded internally, through use of magnetic tape or film, or telemetered to the surface via an acoustic link.

1.11 Telemetering Buoys

Because of limits on available power and practical antenna length, the telemetering or sonobuoy system usually uses a transmitting frequency in the HF or VHF range, in most cases from 27 to 45 Mc/s. Frequently modulation transmission is most common. In some cases an intermediate FM sub-carrier is used, with an amplitude modulated RF carrier signal. The seismic energy is received on a pressure sensitive hydrophone, then amplified, and transmitted back to the receiving ship, where it is recorded on standard recording instruments.

The first telemetering system (Hill, 1952) has been used by the Cambridge group since 1949, with a few modifications in that time (Hill, 1963). A range of up to 45 km. has been achieved with a power output of 3 Watts rf between 40 and 47 Mc/s.

The Dalhousie sonobuoy system (Keen and Loncarevic, 1966) is similar to the Cambridge system, but uses slightly lower frequencies (30 to 40 Mc/s) and lower power output (1.7 Watts rf). Ranges of 30 km. should be possible but as it has been necessary to use a separate recording ship in the vicinity of the buoys, maximum range has not yet been tried.

Defence uses of hydrophone listening systems for submarine detection have led to the development of similar systems by the United States Navy and these have been used on an "expendable" basis by Woods Hole for refraction studies (J. Philips, personal communication). A recent Naval sonobuoy for higher frequency acoustic studies is described by Tetler (1967). Francis (1968) mentions also a Russian sonobuoy system used in the Indian Ocean.

1.12 Recording Buoys

Sonobuoys in use at present are limited by radio range to approximately quasi-line-of-sight distances, not greater than 40 km. Since this is the distance at which mantle energy is just becoming the first arrival, it is most desirable to extend the range to include additional points on a mantle velocity line, especially since radio transmission at this range is weak and the signal-to-noise ratio of seismic signals is poor.

An extended range could be accomplished by increasing the power of the transmitter or lowering the frequency, but both these factors would greatly increase the size and weight of the buoy. A more reasonable solution is to omit the transmission of information and record it within the buoy. This method has been used successfully by a number of groups.

The Cambridge sonobuoy system was redesigned in 1962 (Francis, 1964, Hill, 1963) to utilize an internal galvanometer 35 mm film recorder instead of the transmitter. A radio receiver is used to receive recording commands from the parent ship, turning on the film recorder before the firing of each shot.

Similar systems have been used by the University of Wisconsin (Meyer et al., 1967, Meyer, 1967) and the Graduate Research Center of the Southwest (Green and Hales, 1966). Both of these systems record on magnetic tape. All the systems retain a radio link with the parent ship for starting the recorder.

A system in many ways similar to the one described in this thesis is being developed at Cambridge University (D. McKeowen, C. Keen, personal communications). Both it and the one described in this work are to be used in August, 1968 during a joint Bedford Institute, Dalhousie University, Cambridge University cruise on the Mid Atlantic ridge.

1.12 Ocean Bottom Recorders

Ewing's initial attempts at ocean bottom recording (Ewing and Vine, 1938) were interrupted by World War II. After the war the availability of wartime hydrophone systems led to the adoption of the technique of using shots and receivers near the sea surface, and the ocean bottom method was left dormant. In 1951 the project was renewed when the system described by Ewing and Ewing (1961) was developed.

In 1960 the technique again received attention when the American Government's concern for the detection of nuclear bomb tests led to the financing of three independent studies in ocean bottom recording. The work of Columbia University (Lamont Geological Observatory) (Sutton et al., 1965), Texas Instruments (Schneider et al., 1964), and the University of California's Institute of Geophysics and Planetary Physics (La Jolla) (Bradner and Dodds, 1964) is summarized in two review papers by Bradner (1964a, b). The issue of the IEEE Proceedings in which the paper by Sutton et al. (1965) appears contains a number of other papers on ocean bottom systems. The results have been used for microseism study, earthquake and nuclear blast recording and signal-to-noise ratio measurements, and have provided excellent information on the conditions to be expected on the ocean floor. They are used for frequencies lower than those of interest in explosion studies but could be modified for refraction use.

The Texas Instruments and La Jolla systems are both of the "pop-up" type, i.e. free falling to the ocean bottom and returning to the surface either on command or after a pre-set length of time. Lamont has developed two systems. One is an adaptation of the original Ewing system (Ewing and Ewing, 1961), telemetering information to the surface via an acoustic link. The other is placed offshore, returning data via a cable to land. All these, except the acoustic link system, record directly on magnetic tape and are used at depths of up to 25,000 ft. for periods of up to one month.

The Tokyo University Earthquake Research Institute has also developed a bottom recording unit (Nagumo et al., 1965). Francis (1968) makes brief reference to a recent Russian development. Previous Russian studies on the ocean floor were done by Monakhov (1961) (Bradner, 1964a) in the North Atlantic and the Black Sea.

A sea floor system under development at Cambridge University has been designed especially for refraction studies at sea. The original system (Shorthouse, 1964) used a galvanometer film camera and an array of four hydrophones. It was modified by Whitmarsh (1967) with the addition of a tape recorder and improved transistor circuits. Whitmarsh used a pop-up method with glass spheres for instrument housing and buoyancy, but difficulties with the reliability of the spheres restricted their use to shallow water.

1.2 History of Dalhousie Seismic Studies

Since 1962 Dalhousie University has been involved in a continuing study of the earth's crust and mantle off the eastern seaboard of Canada (Ewing et al., 1966). Specific areas of interest have been the extent of the Appalachian system, the continental margin and the continent-ocean boundary. The first studies (Barrett et al., 1964) used explosives detonated at sea as the energy source. Recordings were made at a number of stations on land using conventional oil industry recording systems. The Dalhousie equipment as described by Barrett (1963) is a Southwestern Industrial Electronics (S.I.E.) very low frequency refraction system originally designed by S.I.E. for use by the U.S. Department of the Interior, Geological Survey, in their Vela Uniform crustal studies.

In 1964 the system was expanded by the introduction of a number of telemetering sonobuoys for use in refraction studies at sea. These buoys, as described by Keen (1966), are modified Canadian Air Force type SSQ-504 sonobuoys, developed by E.M.I. Cossor for use in submarine detection. It had been hoped that these buoys would provide a method of refraction surveying at sea using only one ship for both shooting and recording, but limitations of range, operating time and reliability made it necessary to use one ship for tending the buoys and another for shooting.

In 1966 it was decided to investigate the possibility of developing a more sophisticated recording system for seismic studies at sea. The need was for a self-contained seismic detector, capable of unattended operation during the time necessary for a survey, independent of a second recording ship.

During a sonobuoy refraction experiment off N.E. Newfoundland in 1966 (Fenwick, 1967) a tape recorder was added to the basic Dalhousie sonobuoy system as the first step in the development of a self-contained recording unit. At the same time a geophone was placed on the bottom, in 200 fathoms, and was connected to the recording buoy by an electrical cable. The results were moderately successful, a small number of good records being obtained.

The demands of low power consumption and high stability necessary in remote recording for any great length of time made it obvious that the sonobuoys were not readily adaptable for this application and that the development of a new system was necessary.

The following chapters describe the resulting system. It is a low power, self-contained seismic recording unit specifically designed for use in a surface buoy system at sea. It has been kept small in volume and power consumption with the hope that future developments will lead to the utilization of most parts of the system in a bottom recording unit.

The recorder is useful on land as well as at sea. Since it can be programmed to turn on and off at various intervals, there are many projects that could make use of it in remote operation. The most obvious are sampled study of random events, such as microseismic or earthquake activity, or for the recording of programmed events, such as mining quarry blasts or explosion detonated specifically for seismic studies. Array techniques could be used requiring a limited number of personnel and covering a large area. In general, the system is useful in any study requiring a number of sensors, set to record at specified times, especially where number, size and power make the use of conventional recording systems unsatisfactory.

CHAPTER 2

RECORDING

2.1 Introduction

The seismic recording system described in this thesis can be divided into two main sections, a portable recording system and a laboratory based playback system. The next two chapters will deal with the recording process, the present chapter describing the signal recording techniques and Chapter 3 dealing with the timing and switching arrangements.

A number of considerations governed the design of the recording section. Since it is to be a field operating unit, environmental factors such as temperature range, humidity and acceleration are of great importance. The life of the unit depends on the power consumption and available battery life. Although the desired limits of very low power have not yet been reached, the system is still low power in terms of most commercially available equipment and many of the components could be the fore-runners of a future very low power recorder.

The primary application of the system is as a marine seismic recorder and the possibility of loss of instruments at sea makes low cost another important design factor. The only component to suffer from this restriction is the tape transport. The price difference between readily available commercial recorders and high precision instrumentation recorders restricted the project to high quality commercially available audio recorders. As will be mentioned in Chapter 5, in spite of their disadvantages these recorders performed very well.

In addition to the clock and switching functions described in the next chapter, the recording section consists of the following signal components:

a) Detector

b) Amplifiers

c) Modulators

d) Tape drivers

e) Tape transport

A block diagram of the complete recording system is shown in Figure 1.

2.2 F.M. Recording and Flutter Compensation

The frequencies of interest in seismic studies range from 0 to 20 Hz for land refraction experiments and 5 to 150 Hz for marine work. The low frequency end is omitted at sea because of wave-induced hydrophone noise and the upper limit is increased to include the high frequency content of water wave arrivals. Frequency Modulation recording was chosen as the most convenient method of recording these low frequencies.

The FM system used is of the pulse counting type. As in all FM systems, the recording process consists of converting the amplitude-time characteristics of the information signal into a corresponding change in frequency of an FM carrier

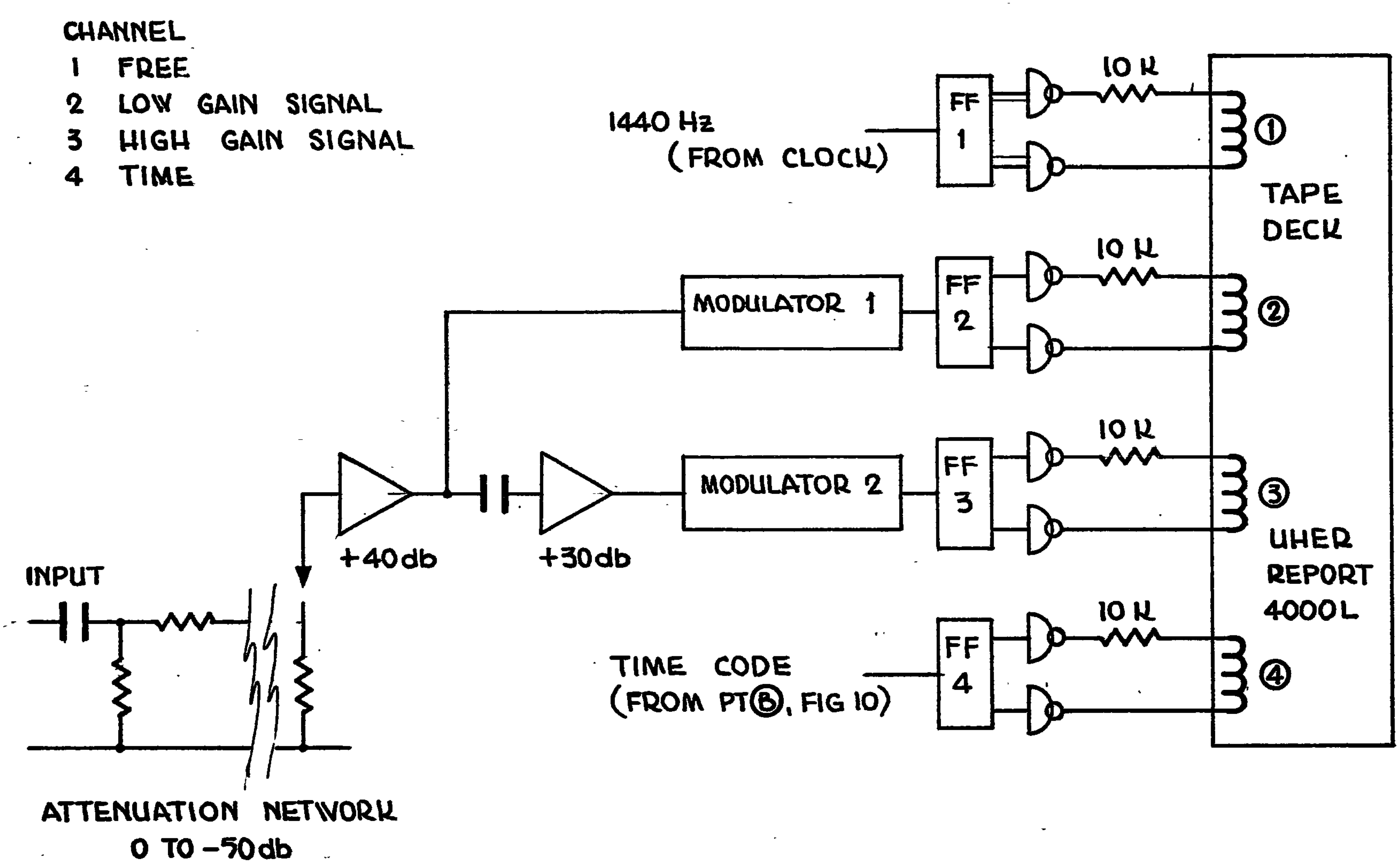


FIGURE 1 RECORD BLOCK DIAGRAM JULY 1968 W.G.M.

signal. The modulator, or voltage controlled oscillator (VCO), gives a constant frequency output for a constant DC input level. A varying signal voltage changes the modulator output frequency in a linear manner. In the modulator used here a more positive voltage level decreases the frequency and a more negative voltage increases the frequency. Thus, for a lower input voltage more cycles of the FM carrier frequency occur in a given time interval.

The frequency modulated signal is recorded on magnetic tape and on playback the FM signal is passed through a demodulator which retrieves the original information signal input. The FM signal is converted into a wave train of pulses of constant width occurring once every cycle of the FM signal. By averaging in a low pass filter, these pulses are, in effect, counted. The more pulses occurring in a given time interval, the higher the demodulated signal output. Since the frequency was made higher for a lower input voltage, there is a 180° phase shift on playback.

The most serious disadvantage of FM recording is the error introduced by variations in tape speed (flutter). This is especially important when the recorder is used in a severe dynamic environment, as in the present application, where it is placed in a buoy on the sea surface. Any speed variations, either on recording or playback, change the apparent frequency as seen by the demodulator. In FM recording this not only affects the time domain but also the amplitude, since the signal-amplitude information has been converted into frequency variations in the FM process.

To compensate for the amplitude variations caused by tape speed fluctuations the following method is used. A constant frequency is recorded on tape and used as an absolute time reference for the FM signals. What is desired at the demodulator output is not a signal proportional to the FM signal as it comes off the tape, but proportional to the signal as it went on the tape.

Let

f = FM frequency

f_{ref} = reference frequency

as recorded and the same symbols with a prime refer to the corresponding frequencies on playback.

In the demodulator

$$V_{out} = \overline{V_{ref}\, T_o f'}$$

where V_{out} = the information signal output

V_{ref} is the height of the pulses in the demodulator

T_o is the width of the pulses in the demodulator

and the bar signifies averaging.

If a reference frequency is recorded and demodulated to give an output inversely proportional to the f'_{ref} then:

$$V = K/f'_{ref}$$

If this is used as the voltage V_{ref} then:

$$V_{out} = KT_o f'/f'_{ref}$$

$$= K' f'/f'_{ref}$$

Since f' and f'_{ref} both vary in the same manner due to tape speed changes, the dependence on the variations is nullified and

$$V_{out} = K'f/f_{ref},$$

the desired dependence.

This, of course, only corrects for amplitude changes and has no effect on the frequency changes in the signal output due to speed variations.

Further description of the V_{ref} demodulation process will be given in Chapter 4.

2.3 Recording System Components

2.31 Detectors - For marine seismic use the detector is the same hydrophone as that used with the Dalhousie sonobuoys. The hydrophone itself is an expoxy enclosed piezoceramic cylinder and is suspended on a 100 foot neutrally buoyant cable section, which floats 200 feet below the surface (see Keen, 1966). A pre-amplifier (Fyfe, 1967) with a gain of 30 db is included at the hydrophone end of the cable. The pre-amplifier output for ambient sea noise levels is in the order of 100 μV. (C.Keen, 1968, personal communication).

2.32 Amplifiers - To increase the dynamic range, two levels of signal, separated by 30 db, are recorded. The amplifier circuit is shown in Figure 2. Use has been made of the Nexus Q-200 operational amplifier. These amplifiers are especially suited for application in the present system, having the very low quiescent current drain of 50 μamps, and good temperature stability and noise figure.

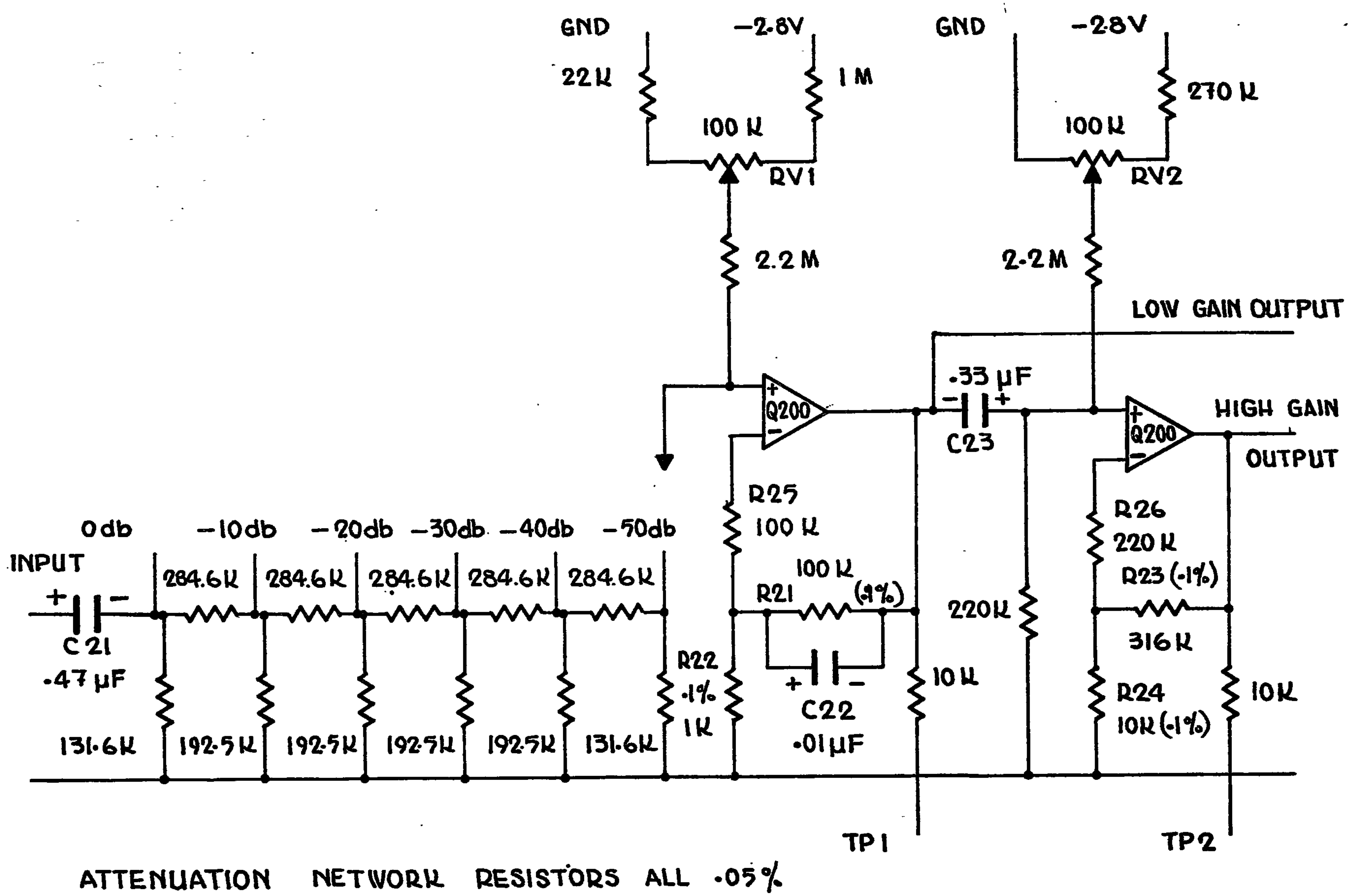


FIGURE 2 | RECORD AMPLIFIER | JULY 1968 W. G. M.

The first amplifier stage A_1 has a gain of +40 db, defined by the feedback network R_{21} and R_{22}

$$\frac{R21}{R22} = \frac{100\ K}{1\ K} = 100 = 40\ db$$

The maximum gain is set by the ratio of these two resistors and it can be changed, if desired, to give a higher gain. For example, changing R_{11} to 1 Megohm gives a gain of 60 db.

The resistor network preceding A_1 is a constant impedence attenuator providing an input impedence and source resistance of 100 K, independent of the attenuator setting. The input can be attenuated from 0 db to 50 db in 10 db steps. Since the constant source resistance means that the input noise due to thermal resistive noise will be constant, the lower attenuation settings should be used whenever possible to improve the signal to noise ratio.

The second stage amplifier A_2 has a gain of 30 db,

$$\frac{R23}{R24} = \frac{316\ K}{10\ K} = 31.6 = 30\ db$$

The frequency response is determined by capacitors C_{21}, C_{22} and C_{23}. In preliminary experiments at sea it was found that large amplitude low frequency noise in the order of 1 Hz was induced into the hydrophone system by wave motion. The capacitor C_{21} provides for a low frequency cut-off of 6 db per octave below the 3 db point of 4 Hz on the low gain channel. The capacitor C_{23} adds an additional roll off of 6 db per octave producing 12 db per octave below 3 Hz on the high gain channel. The capacitor C_{22} provides a high cut-off of 6 db per octave above 150 Hz. The gain characteristics of the amplifiers is shown in Figure 3.

As will be explained in the next section, the modulators require a -1 Volt offset on the input signal. The two offset trim resistors Rv_1 and Rv_2 are provided for this purpose. The outputs of the two stages are brought out through the test points TP1 and TP2.

The temperature stability of operational amplifiers is improved if the resistance from each input to ground is the same, so that the leakage currents are offset by equal voltages at the differential inputs. For this reason the resistors R_{25} and R_{26} are inserted in the inverting inputs and have the same value as the resistance to ground from the non-inverting input.

2.33 <u>Modulators</u> - The initial design of the modulators described in this section was undertaken as a summer research project at the Bedford Institute (Fitzgerald, 1967).

An FM modulator or voltage controlled oscillator (VCO) provides an output frequency proportional the input voltage. The modulator shown in Figure 4 performs this operation in the following manner. The input stage is an integrator which, given a constant DC input, produces a ramp function. When the ramp function reaches 1.4 Volts the comparator fires, triggering the one-shot. The one-shot output is transformer coupled to a switch across the integrating capacitor C_{41} of the input stage, which is discharged as the one-shot fires, returning the integrator output to zero. An output pulse is thus produced each time the integrator

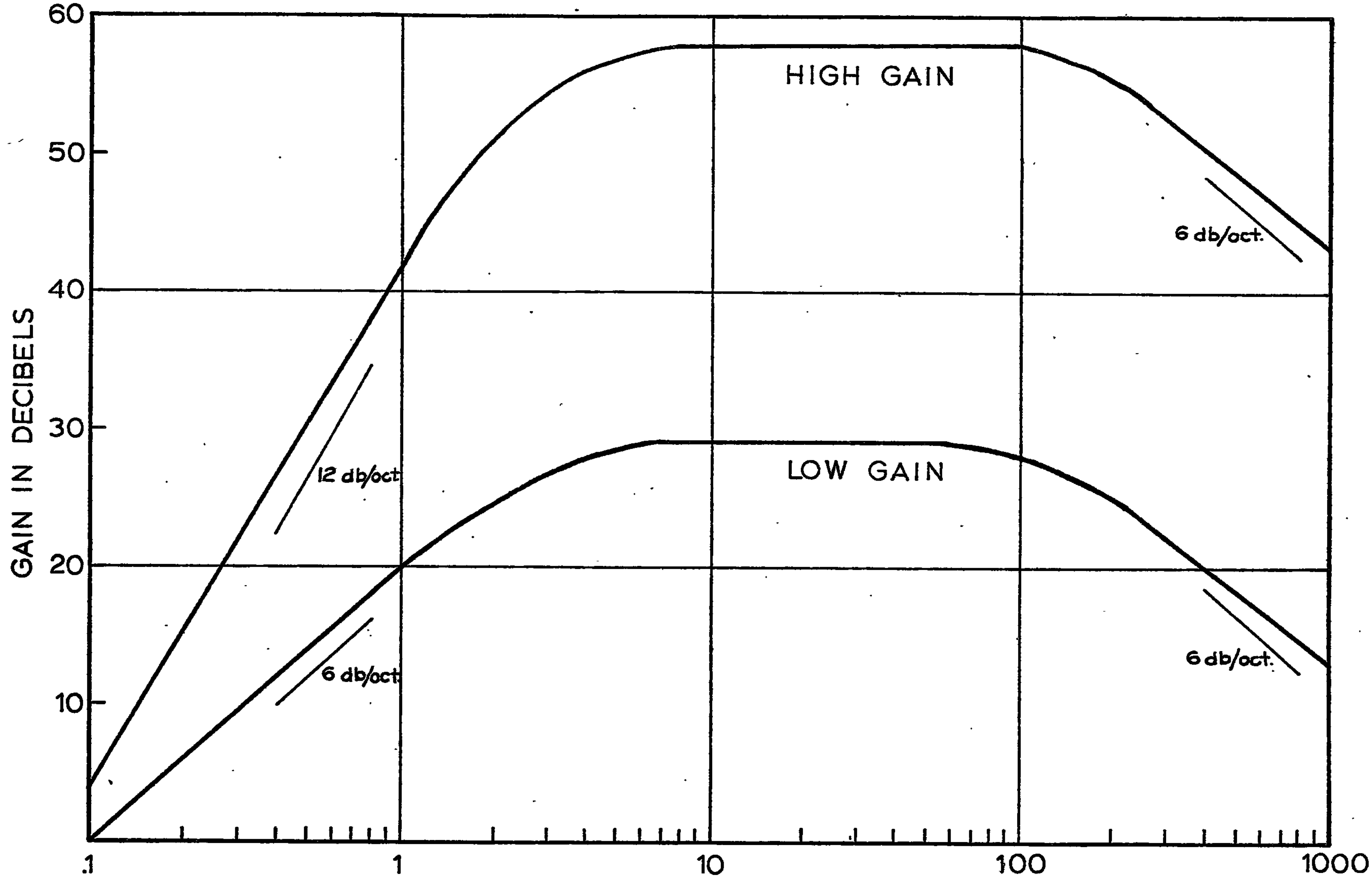
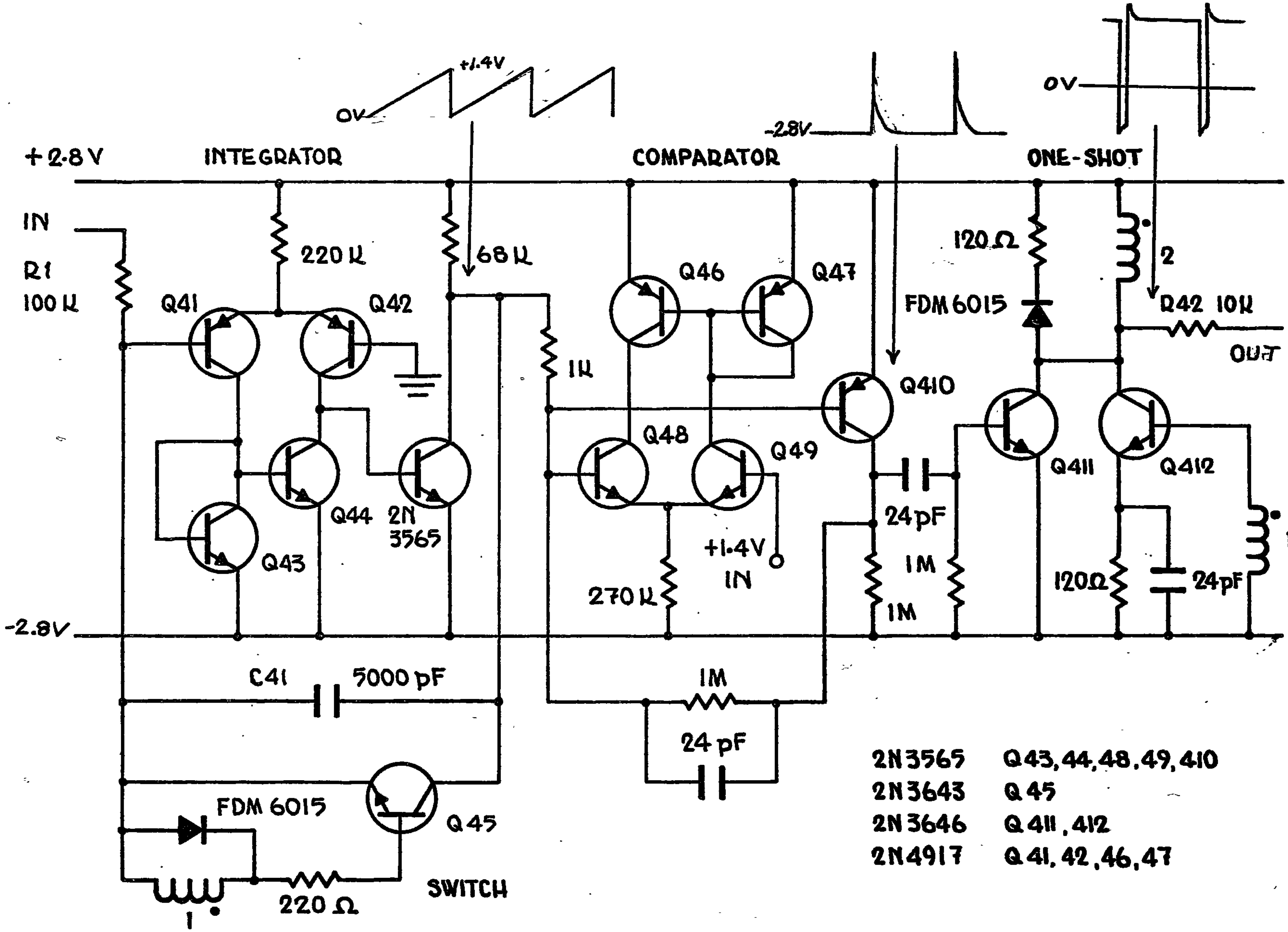


FIGURE 3 AMPLIFIER GAIN



2N3565	Q43, 44, 48, 49, 410
2N3643	Q45
2N3646	Q411, 412
2N4917	Q41, 42, 46, 47

FIGURE 4	MODULATOR (V.C.O.)	JULY 1968 W.G.M.

reaches 1.4 Volts. The slope of the ramp function is proportional to the value of the input voltage and the time necessary to reach 1.4 Volts thus depends on the value of the input voltage. The pulses from the integrator are used to trigger the tape driver which is a flip flop so that the frequency of the modulator is halved.

The usual standard for single channel FM recording is to have a center frequency five times the highest desired signal frequency. Since marine seismic frequencies can be as high as 150 Hz, a center frequency of 750 Hz was chosen. Using the lowest speed on the tape deck of 15/16 ips the packing density is

$$750 \frac{\text{cycles}}{\text{second}} \times \frac{16}{15} \frac{\text{seconds}}{\text{inch}} = 800 \text{ c/in.}$$

and is approximately the IRIG standard of 900 cycles per inch (1.1 mil. wavelength).

Because of the flip flop tape driver the center frequency at which the modulator operates is twice this or 1500 Hz, although the center frequency as it goes on tape is still 750 Hz.

The <u>integrator</u> is simply a differential DC amplifier with capacitive feedback through C_{41}. This amplifier incorporates the usual emitter coupled differential configuration but the customary load resistors in the collectors of the long tail pair Q_{41} and Q_{42} have been replaced by transistors Q_{43} and Q_{44} . These act as equal current sources to ensure that the two branches of the long tail pair are balanced. The bases of Q_{43} and Q_{44} are connected together and Q_{43} is held in the on state by tying its base to collector. Assuming the transistors are identical, equal base currents will flow and hence equal collector currents, holding the currents in the two sides of the differential amplifier equal. The same amplifier configuration is found in the next section of the modulator and also in the playback demodulators.

The time constant of the integrator is set by the RC combination $R_{41}C_{41}$. The output of the integrator is

$$v_{out} = \frac{1}{RC}\int_0^t v_{in}\,dt$$

$$= \frac{1}{RC} v_{in} t$$

and this reaches 1.4 Volts for each cycle of the modulator output.

For a modulator center frequency of 1500 Hz (FM center frequency of 750 Hz) values of 100 K and 5000 pf were chosen for $R_{31}C_{31}$. The nominal DC input v_{in} is, therefore:

$$v_{in} = \frac{v_{out}\ RC}{t} = \frac{1.4\ V \times 10^5\Omega \times 5\times10^{-9}f}{6.6 \times 10^{-2}\ sec.}$$

$$= 1.05\ \text{Volts.}$$

The signal is applied to the inverting input of the integrator and therefore a -1.05 volt input signal gives the center frequency of 750 Hz. This is the reason for the DC offset mentioned in the last section.

The $R_{41}C_{41}$ combination is a Balco matched temperature coefficient network type RC2613

The comparator is the same differential amplified as in the integrator, with a slight positive resistive feedback. The inverting differential input Q_{49} is held at +1.4 Volts so that when the other input, the ramp output of the integrator, reaches this value, the differential output of the amplifier (Q_{410}), originally at -2.8 Volts, goes positive.

The positive pulse triggers the one-shot. The one-shot is a monostable blocking oscillator. The blocking oscillator circuit is used since it supplies the short, high current pulse necessary to drive the switch Q_{45} and quickly discharge the capacitor C_{41}. The pulse length (in the order of 4 μsec.) must be short and of constant width so as not to effect the frequency of the modulator. The transformer in the blocking oscillator is Indiana General Feramic Torroid wound with number 32 wire in the ratio 2:1:1 (60:30:30 turns).

The output pulse from the one-shot is used to trigger the flip flop tape driver. The 10 K resistor R_{42} is inserted in the output line to limit the current drive to the flip flop. When not driving the flip flop the power consumption of the modulator is 250 μamps from both the plus and minus 2.8 Volt supplies, and when driving the flip flop the drain on the +2.8 Volt supply increases to 500 uamps. (Without the 10 K resistor it is as high as 5 mA.)

2.34 Tape Transport and Heads

The tape transport is a Uher 4000 Report L, 4-speed tape recorder. The lowest speed of 15/16 ips has been used. The recorder holds 5 inch reels and allows for 180 minutes recording on 1 mil tape, or 240 minutes on .5 mil tape. The Uher is supplied with half track, single channel heads and these have been replaced with Nortronics type 5603 miniature 4 channel heads. These heads are a high impedence laminated core type and, as the next section shows, give a reasonable output for saturated recording signals.

2.35 Tape Drivers

Because of the advantage of their bi-directional output, flip flops have been used to drive the tape heads as shown below:

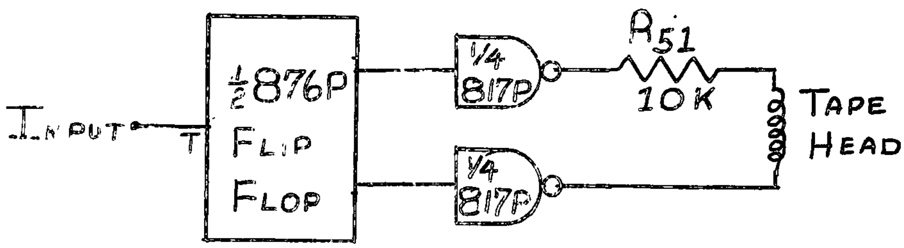


Figure 5. Tape Driver

The two gates are used as buffers to provide the necessary current to drive the heads. (See Appendix 1 for a discussion of flip flops and gates.) Since the flip flop is a bi-stable element, providing both positive and negative outputs, current is driven in both directions through the heads, ensuring saturation in each phase of the cycle.

The value of the resistor R_{51} was chosen to give the optimum record current, for saturated recording, over the frequency range of interest. Below the optimum current full saturation is not achieved and above this value a self erasing field is set up. Both these cases lower the output voltage available on playback. A graph of output vs frequency and value of R_{51} is shown in Figure 6. This was made using the set-up shown in Figure 5 and Ampex type 641 magnetic tape. The value chosen for R_{51} was 10 K.

It must be remembered that using a flip flop halves the frequency of incoming signals, so that the output of the modulators and clock information must be twice the frequency that is desired on tape.

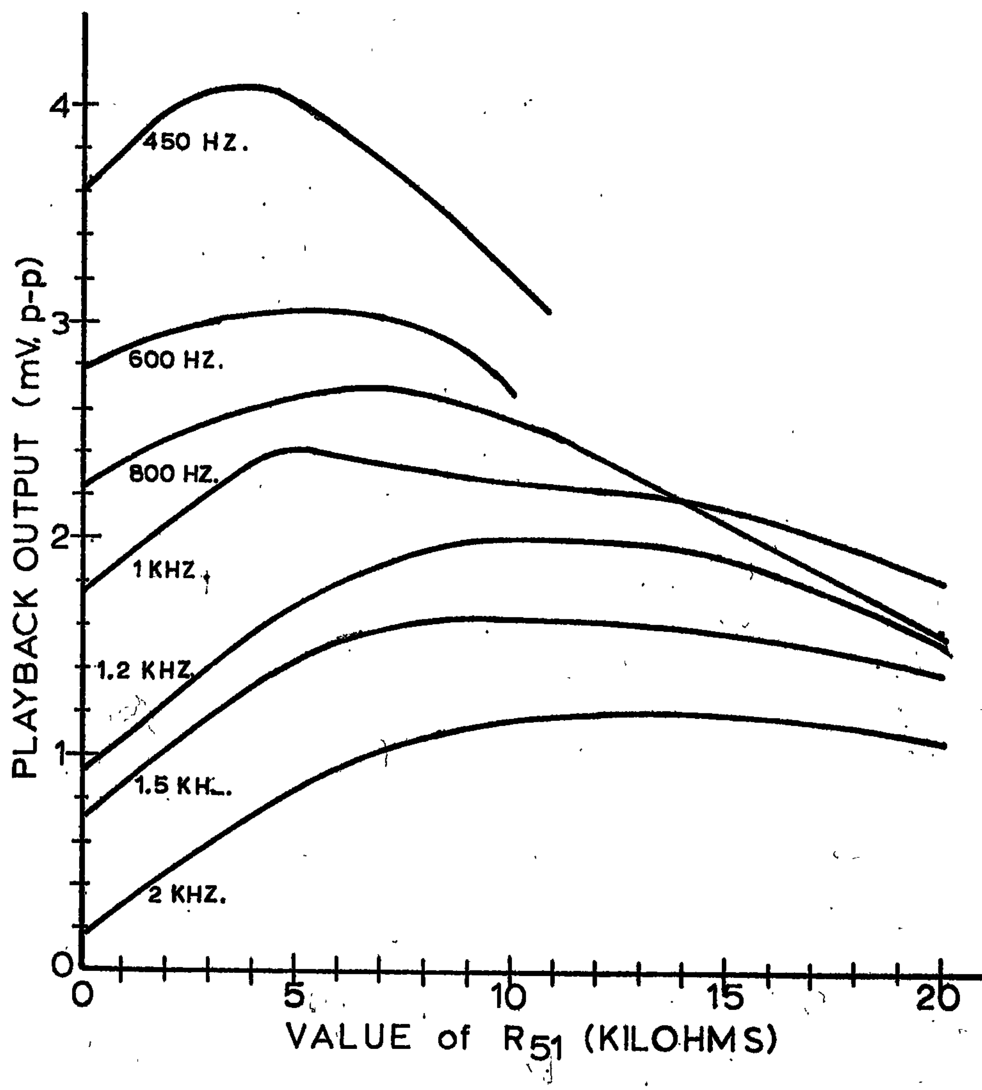


FIGURE 6 TAPE RESPONSE

CHAPTER III

THE CLOCK

3.1 Introduction

The clock has been perhaps the most important and novel part of this system. For seismic refraction studies the travel time of energy from source to receiver must be known to one hundredth of a second or better. In conventional studies this is achieved by either recording, at the receiver, a shot instant transmitted from the source via a conductor or radio link, or recording a common absolute time (e.g., from radio stations W.W.V. or C.H.U.) at both the source and receiver. Both these methods have been used in buoys at sea (see Green & Hales, 1966).

When a shot instant is used, the arrival of seismic energy after the shot is timed using a chronometer or timing lines generated within the recorder. Since the exact time of the shot is known the chronometer or timing lines must give the required accuracy of .01 sec. only until the arrival of the energy which is usually less than 1 minute. The accuracy of the type of clock considered here must retain the accuracy over a much greater length of time.

It was realized that if the present system was to be truly remote and used on the ocean bottom or beyond the range of radio reception, the use of an external time source would not be possible and an internal standard of sufficient accuracy would have to be developed.

Stability of the degree required can be achieved by using a high frequency oscillator with a high stability quartz crystal as the standard. This standard frequency is then divided electrically in a number of stages to give pulses of the required nature, in the present case ranging down to one pulse per day. The clock is, in effect, a counter arranged to go through a complete cycle in one day. The outputs of the stages from 1 pulse per .1 minute to 1 pulse per day are in a binary coded decimal (B.C.D.) format, i.e. giving a B.C.D. count of the tenths of minutes, minutes, tens of minutes, hours and tens of hours. These outputs can be decoded to show the state of the clock at any time, or in other words the portion of a day it has counted through or "the time". This decoded information can be displayed on decade readout tubes (NIXIE tubes) to give a visual display of the time. Before being placed in remote operation the clock can be set by speeding up the counting rate until the output corresponds to the time as given by the standard being used and then letting it return to its normal rate. The recorder then has its own internal time source that corresponds to the time at the master station. The record programming and the arrival of seismic energy can be timed relative to this source.

The function of the clock is two-fold. It must supply timing information to be recorded on tape with the seismic signals and must also control the instrument, by turning the recorder on and off at pre-determined times. The timing information consists of pulses every second and a coded count of the hour at the start of each record. The controlling function consists of the logic necessary to determine the on and off times and a relay to start and stop the tape transport.

Four main sub-systems are included in the clock:

1) The main clock itself providing outputs down to one cycle per day
2) The timing system for coding time information on tape
3) The logic and switching networks for controlling the recorder
4) A laboratory-based readout for visual display of the time.

3.2 The Main Clock

3.21 Crystal and oscillator - The required life of the system during a typical refraction experiment at sea is usually less than four days. The stability necessary is, therefore:

.01 seconds in 4 days

.01 seconds in 3.4×10^5 seconds

or 1 part in 3.4×10^7

or approximately .03 parts per million.

The crystal oscillation that was finally chosen is a Model 562 TXCO Plastipac Oscillator manufactured by Gibbs Manufacturing and Research Corporation. The output is a 3 Volt peak square wave at 184.32 KHz. The unit has a power drain of <30 mW. The stability over the temperature range encountered on the sea surface does not quite meet the figure above. A discussion of the clock stability will be found in Chapter 5.

As described by Gerber and Sykes (1966), the frequency of a crystal oscillator changes because of two main reasons. Long-term stability of the crystal is affected by the rate at which the crystal material ages. Short-term stability is governed largely by changes in temperature affecting the properties of the crystal. The short-term temperature variation usually predominates and is the more important in the present application. The problem of temperature variation is usually overcome by placing the crystal in an electric oven, in which the temperature is kept constant to within a few tenths of a degree. In the present system, the limitation on power made it impossible to consider using an oven, since most require well over .5 watts. The absence of an oven is not as severe as it may first appear. Although the present system operates from a buoy on the sea surface and is subject to diurnal change in temperature, future developments could take advantage of the excellent constant temperature environment provided by the sea. Temperature variations at a given place on the ocean floor are believed to be less than .005°C and even submerging the unit a few meters below the sea surface keeps the temperature constant to within .1°C (see Defant, 1961, p. 109). On land the unit could be buried in the ground to provide a stable temperature environment. Burial of about one meter attenuates the temperature variations on the surface by a factor of .002 and daily variations of 15°C would appear as a change of only .03°C (see Jaeger, 1965).

3.22 <u>Theory of Operation</u> - In order that the oscillator output may be used as the reference for a timing unit, the frequency is divided by a counter system down to one cycle per day. The division is accomplished by using "flip-flops" (binary dividers or bistable multivibrators). The flip-flop is basically a divide-by-two unit; i.e., for every two input pulses, one output pulse is given. By connecting n units in a chain, the output of one connected to the input of the next, division by 2^n can be accomplished. Various feedback networks can be used to divide by any factor, giving an output pulse for a pre-determined number of input pulses. The basic action of a flip-flop and the feedback networks for the division ratios of interest (divide by 3, 5 or 24) are described in detail in Appendices 1 and 2. An 8-4-2-1 B.C.D. code is used throughout. Using the simple divide by 2 and the more complicated divide by 3, 6, and 24 networks, the clock is arranged as shown below:

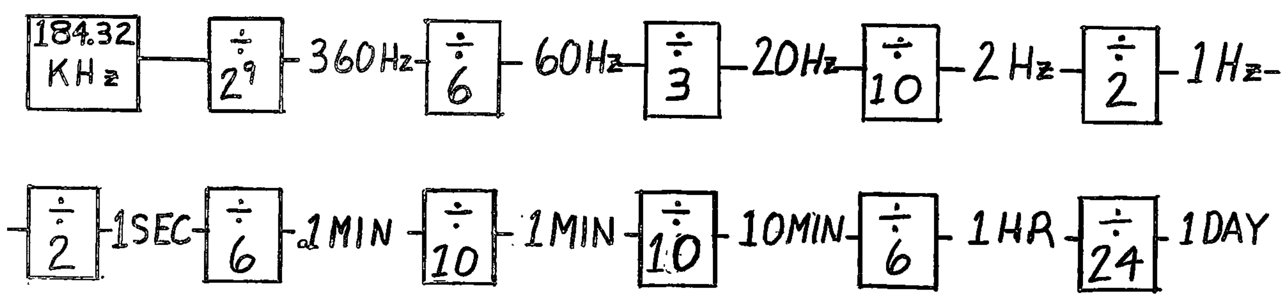


Figure 7. Clock Block Diagram

Note that a divide by 6 is simply a cascade of a divide by 2 and divide by 3, and a divide by 10 is a divide by 2 and divide by 5. The complete interwiring diagram is shown in Figure 8.

All the outputs of the clock are brought to one 24 pin connector. The various outputs and their pin numbers are listed in Table 1. All the BCD outputs are available from .1 minutes to 20 hours as well as 1 Hz, $\overline{\text{1 second}}$ and $\overline{\text{4 seconds}}$ for timing purposes, and 1440 Hz for the reference frequency channel and timing circuits.

3.23 <u>Components</u> - The initial stage of this project was spent in trying to develop very low power flip flops using discrete components. A number of circuits were tried but did not achieve the reliability necessary for the system. The two main problems were associated with low temperature performance and noise immunity. One unit had a power dissipation of less than 50 μwatts per flip flop but failed to meet the specifications at low temperature (<5°C.) and was easily triggered by external noise sources, such as switching relays. Development is continuing at the Bedford Institute on low power units.

The Motorola line of low power plastic mWMRTL digital integrated circuits were finally chosen after consideration of power consumption and cost. A few other lines are available at slightly lower power but cost is greater by a factor of ten or more. Four different units are used in the clock and all are in plastic dual-in-line packages and cover the temperature range of 0°C to +75°C. The MC876P is a dual

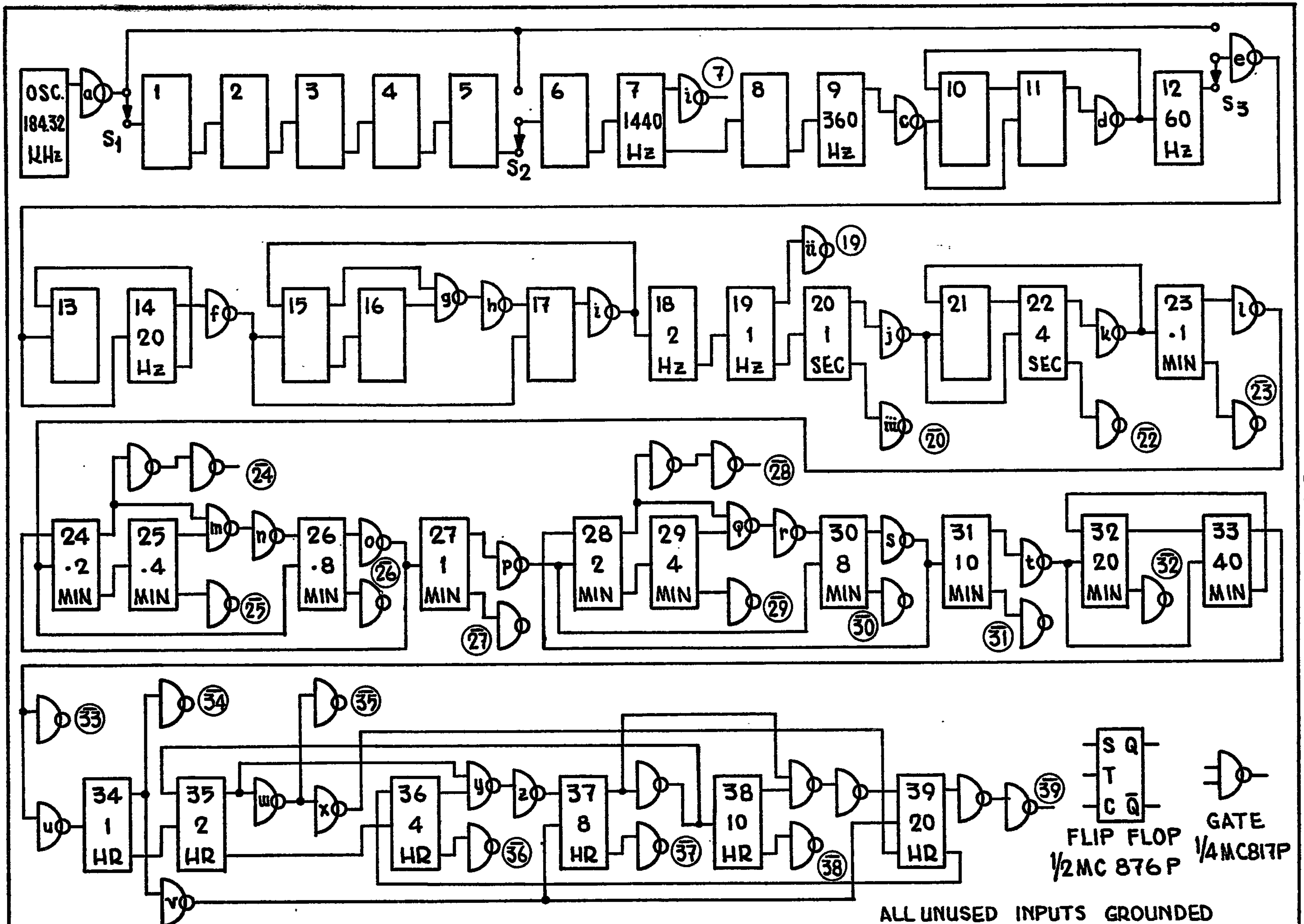


FIGURE 8 — THE CLOCK — JULY 1968 W.G.M.

TITLE	FF No	PIN No
$\overline{\text{20 HR}}$	39	19
$\overline{\text{10 HR}}$	38	18
$\overline{\text{8 HR}}$	37	17
$\overline{\text{4 HR}}$	36	16
$\overline{\text{2 HR}}$	35	15
$\overline{\text{1 HR}}$	34	14
$\overline{\text{40 MIN}}$	33	13
$\overline{\text{20 MIN}}$	32	12
$\overline{\text{10 MIN}}$	31	11
$\overline{\text{8 MIN}}$	30	10
$\overline{\text{4 MIN}}$	29	9
$\overline{\text{2 MIN}}$	28	8
$\overline{\text{1 MIN}}$	27	7
$\overline{\text{.8 MIN}}$	26	6
$\overline{\text{.4 MIN}}$	25	5
$\overline{\text{.2 MIN}}$	24	4
$\overline{\text{.1 MIN}}$	23	3
1 HZ	19	20
$\overline{\text{1 SEC}}$	20	21
$\overline{\text{4 SEC}}$	22	22
1440 HZ	7	23
+4 VOLTS		2
GROUND		1

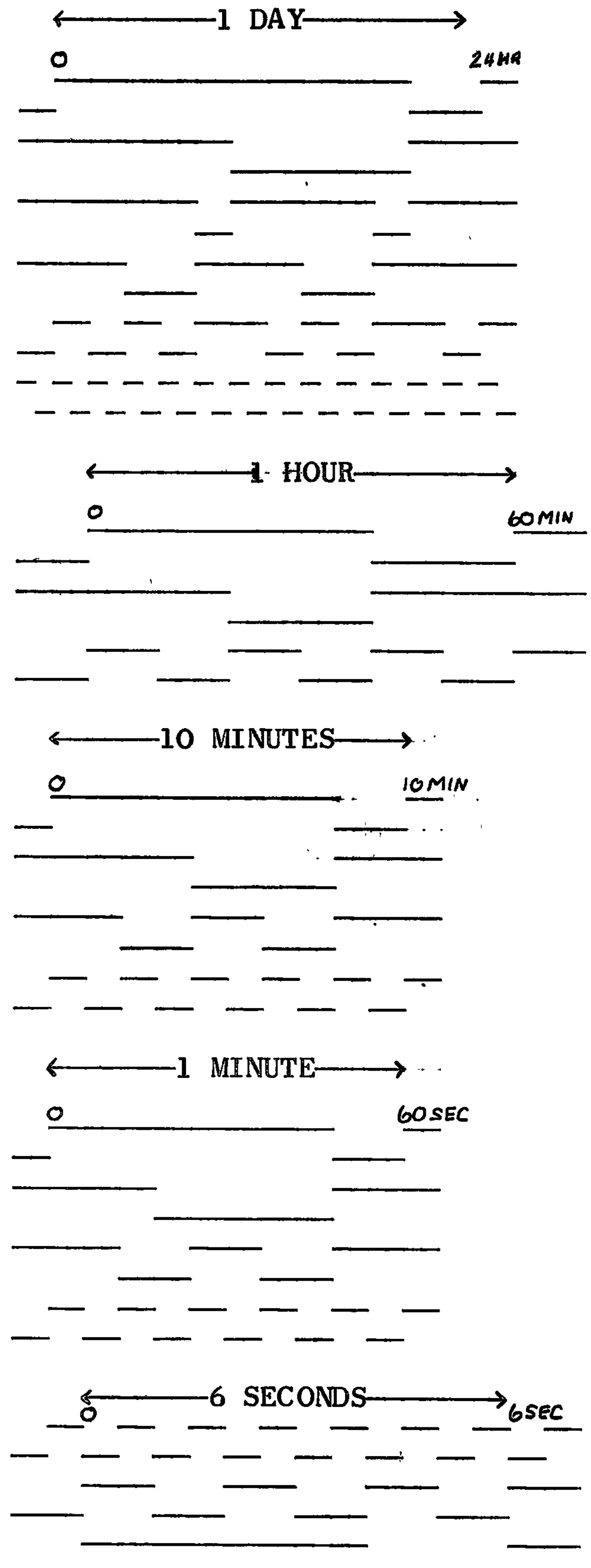


TABLE 1 CLOCK OUTPUTS

JK flip flop and requires 20 mW per flip flop. The MC817P contains four 2-input NAND/NOR gates and the MC819P two 4-input gates. Each requires approximately 3 mW per gate. The action of each of these units is described in Appendix 1.

3.3 Readouts

Two units are available for displaying the time. The low power clock has been made compatible with the Bedford Institute Master Clock so that all that is needed is a buffer unit to use the Master Clock readout to display the low power clock output. A portable battery operated unit has also been designed for field use.

The readout is not an integral part of the recording system and is only used when setting the clock or as a visual time display in the lab.

The Bedford Institute Master Clock has been developed for shipboard and laboratory use by Dr. A.S. Bennett. A buffer unit is necessary to change the logic levels and provide the current necessary to drive the Master Clock. The logic levels for the low power clock are:

1 = .8V   0 = 0 V

and for the Master Clock they are

1 = 0 V   0 = -5 V.

The buffer circuit is shown in Figure 9. One buffer is needed for each of the clock outputs from .1 minutes to 24 hours.

For portable field use a separate miniature readout has been designed using Fairchild CuL9960 micrologic integrated

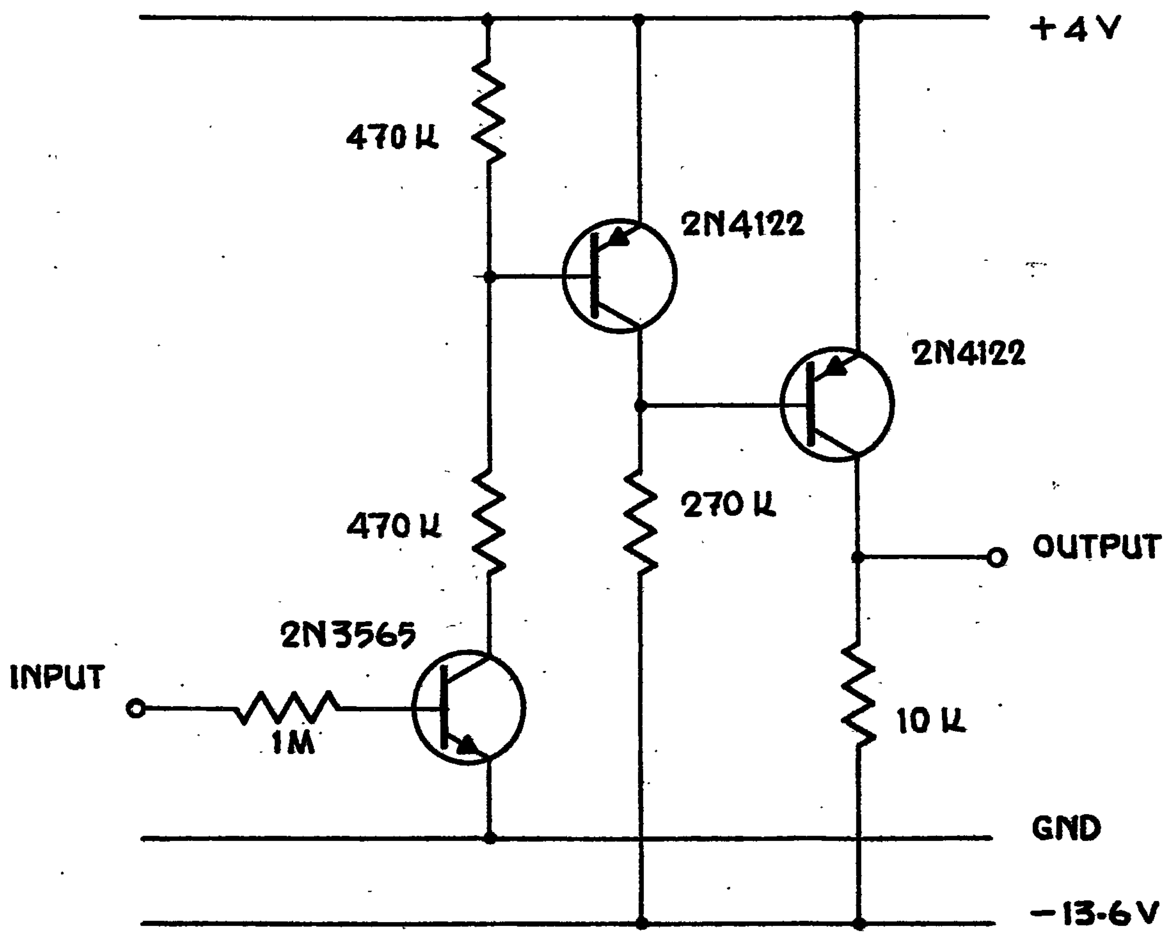


FIGURE 9 | CLOCK BUFFER | JULY 1968 W.G.M.

decade decoders and miniature Burroughs 7977 (B4032) NIXIE tubes. Two 90 Volt radio batteries (Mallory M214) are used to provide the anode voltage for the readout tubes.

3.4 Time Code

The time information recorded on tape consists of the following:

a) .2 second pulses every second

b) .5 second pulses every 6 seconds

c) 1.6 second pulses every minute

d) a BCD code, during the first seven seconds of each record, of the hour in which a record was made.

Each record thus contains a continuous series of second pulses, with an obvious minute and six second identification and a code of the hour in which the record was made. Two records occurring during the same hour will have the same hour code, but since most large marine refraction experiments are limited to less than one shot per hour due to charge size and handling problems, this does not present a problem. Even if the recorder has been set to record more than once per hour, it is only a matter of finding the first record with the desired hour's code and playing through the records in that hour until the desired one is reached.

The pulses are recorded on tape by doubling the FM center frequency for each pulse. When demodulated these appear as two different DC levels. Thus the seconds code consists of bursts of 1440 Hz, .2 seconds long every second on a channel which is nominally 720 Hz.

The timing circuit shown in Figure 10 has four main parts:

a) A frequency doubler consisting of gates G_1 to G_5.

b) A time code input consisting of gates G_6 to G_9

c) A shift register consisting of gates G_{10} to G_{16} and flip flops FF_1 to FF_8

d) A one-shot consisting of transistors Q_{101} to Q_{103}.

The input of 1440Hz to the frequency doubler is derived from the clock output $\overline{7}$. The .002 µF capacitor differentiates the input and gives a positive going pulse on the leading edge and a negative going pulse on the trailing edge of each cycle of the 1440 Hz input signal. Since the input of gate G_2 is held positive by the 100 K resistor it is nominally on (output low) and is pulsed off on the negative going pulse or trailing edge of the 1440 Hz signal. The opposite is true for gate G_3. It is pulsed on at the positive going pulse or leading edge of the input signal. If gate G_5 is inhibited (any input positive) only the pulses from gate G_2 will reach G_4 and the output to the tape driver is 1440 Hz. If, however, G_5 is enabled (i.e., all other inputs at ground) then the outputs of gates G_2 and G_3 both reach G_4. They are 180° out of phase, and the output is 2880 Hz. Since the tape driver is a flip flop the frequency is halved and the signal on tape is either 720 Hz or 1440 Hz.

The output of the frequency doubler thus remains at 720 Hz as long as either of the inputs 2 or 3 of gate G_5 is positive and goes to 1440 Hz if they both are at ground. The

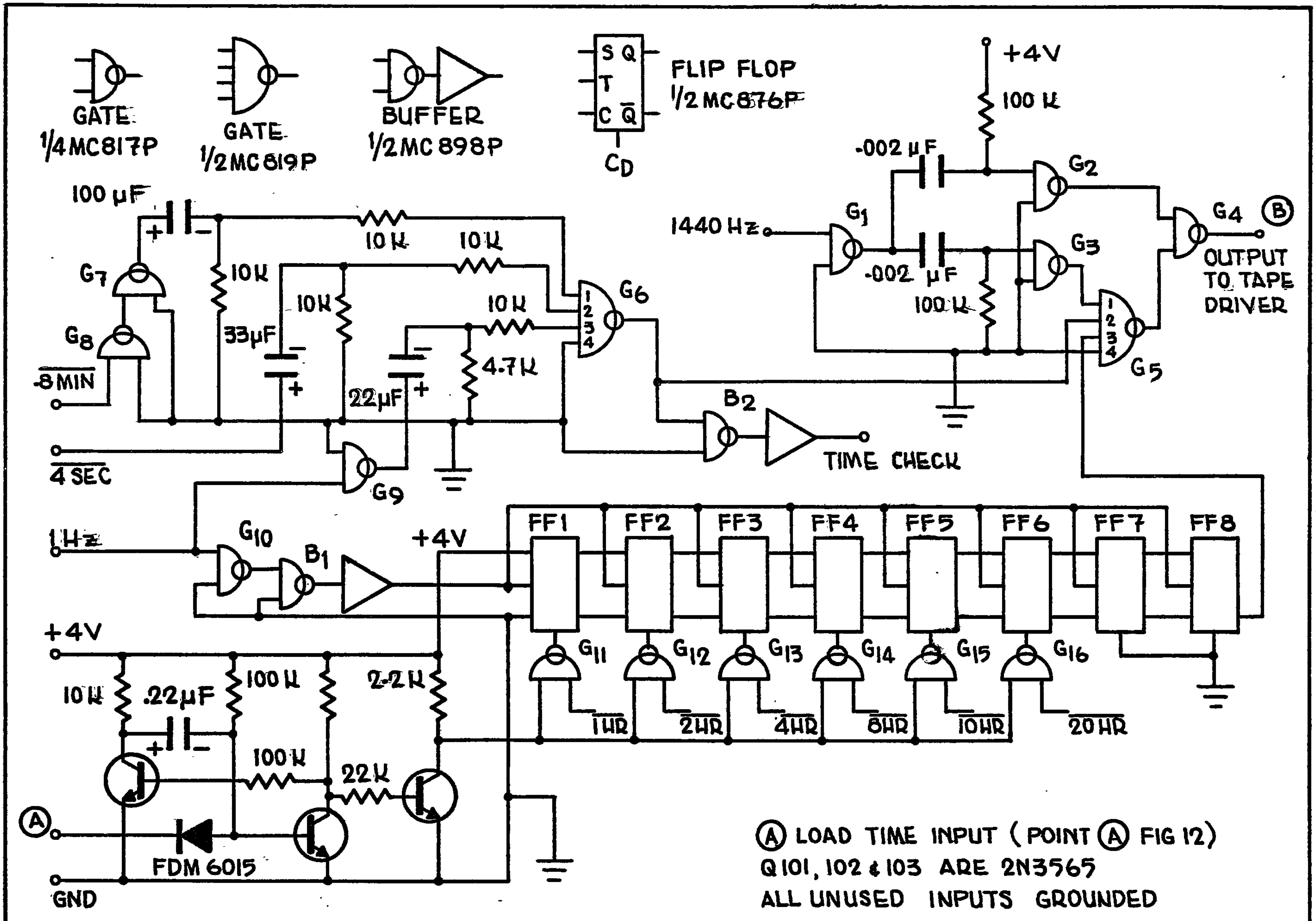


FIGURE 10 | TIMING | JULY 1968 W.G.M.

output of the shift register is nominally at ground so that the time code is usually determined by the state of input 2 of G_5, i.e., the output of G_6. Each of the inputs 1 to 3 of G_6 is an RC network designed to give pulse widths of the times indicated at the start of this section. The inputs of gate G_6 all have pull down resistors to ground so that gate responds to positive going level changes at the inputs of the RC networks. These occur each second at input 1, each 6 seconds at input 2, and each minute at input 3. The inputs are all nominally at ground and the output of gate G_6 is thus usually positive and goes to ground whenever an input pulse occurs, doubling the frequency at the output of gate G_4.

The shift register (FF_1 to FF_8 and G_{10} to G_{16}) is used to provide a code of the hours at the beginning of each record. Following the action of the flip flop described in Appendix 1, the 1 Hz signal from gate G_{10} triggers the chain of flip flops each second and loads the Q and $\overline{Q}$ state of each flip flop into the next one. The output of the one-shot (Q_1 to Q_3) is usually at a positive logic level, so that all the C_D inputs of the flip flops are at ground. Since the S and C inputs of FF_1 are at +4V and ground respectively, the Q output shifted through the register is usually a logic 1 and the $\overline{Q}$ level is at 0.

The one-shot is triggered by the same signal that turns on the tape recorder and it has an on time of approximately 20 msec. When the one-shot is triggered its output goes to ground, the gates G_{11} to G_{16} are all enabled and the force clear (C_D) inputs to all the flip flops take on the inverse of the hours inputs ($\overline{\text{1 hour}}$ to $\overline{\text{20 hour}}$) that are present. If this is the case the flip flop outputs are forced into the state defined by the C_D input and these levels are shifted through the register.

For example, if the record occurs during the 20th hour the $\overline{\text{20 hour}}$ input is at ground and the rest are all at a positive logic level. The force clear input (C_D) of flip flop FF_6 is positive and this flip flop only is forced into the clear state ($Q = 0$, $\overline{Q} = 1$). The command pulse that turns the recorder on triggers the one-shot and forces FF_6 into the clear state. At the same time the 1 Hz signal from gate G_{10} shifts the clear state into FF_7. The first second after the on command shifts the clear state into FF_8 and on the second second the high $\overline{Q}$ state arrives at input 3 of gate G_5. This inhibits the frequency at G_4 from doubling and no second pulse occurs. If any of the other hours inputs had been present they would appear at the gate G_5 during the relevant second after the on command.

The seconds 2 to 7 after the recorder turns on are thus weighted by the BCD weights 20 hours to 1 hour as shown below.

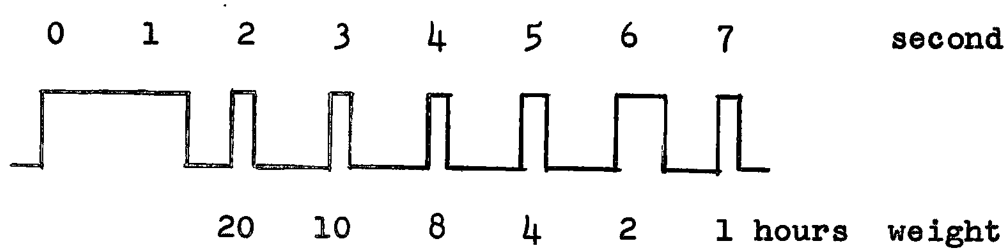


Figure 11. Hours Time Code

For those hours for which the BCD code is 1 the second pulse will be inhibited from appearing. The time can be found by simply adding together the weights of those positions in which a pulse does not appear.

3.5 Switching

In addition to providing time information, the clock is used to control the record programming of the system. Since the time between records and the recording time necessary depends greatly on the experiment, it is necessary to provide various recording lengths and intervals.

All the BCD outputs from .8 minutes to 2 hours have been made available for switching the recorder on and off. These are listed in Table 2.

To conserve power a magnetic latching relay has been used. It has two coils and a latching magnet so that only a short pulse through one coil is necessary to pull the relay on, and a pulse across the other coil to turn it off. The coil resistance is 25 Ω and it requires 6 Volts for approximately 20 msec. to ensure full switching. The one-shots used to provide the pulses are shown in Figure 12. In the "on" one-shot it was found that a longer pulse (40 msec.) was needed since the tape recorder, which runs off the same supply, draws such a large current when turning on, that the full 6 Volts is not available for switching the relay. The extra transistor Q_{123} in the "off" one-shot is added so that current is drawn in the "off" coil of the relay, only when the relay is already on. When in the off

Pin (see Plate 6)	Title	Derived from Output of FF No.	Switching Pulse Occurs
1	ON		
2	OFF		
3	.8 min	25	on 48 seconds after each minute
4	1 min	26	on every minute
5	2 min	27	on every even minute
6	4 min	28	at 4, 8, 14, 18, 24, 28 ... 54, 58 minute after each hour
7	8 min	29	at 8, 18, 28, 38, 48, 58 minute after each hour
8	10 min	30	on the hour and every 10 minutes after the hour
9	20 min	31	on the hour and every 20 minutes after the hour
10	40 min	32	at 40 minutes after the hour
11	1 hr	33	on every hour
12	2 hr	34	on every even hour

To set the time for the recorder to turn on, jump a wire between Pin 1 and the pin for the desired on time.

To set the time for the recorder to turn off, jump a wire between Pin 2 and the pin for the desired off time.

Example: Pin 1 to Pin 9 and Pin 2 to Pin 4 will record for one minute on the hour and at 20 and 40 minutes after the hour.

Pin 1 to Pin 7 and Pin 2 to Pin 6 will start at 8 minutes after the hour and record for six minutes, turning off at 14 minutes after the hour. It will also record for six minutes at 18, 28, 38, 48 and 58 minutes after the hour.

TABLE 2. SWITCHING TIMES

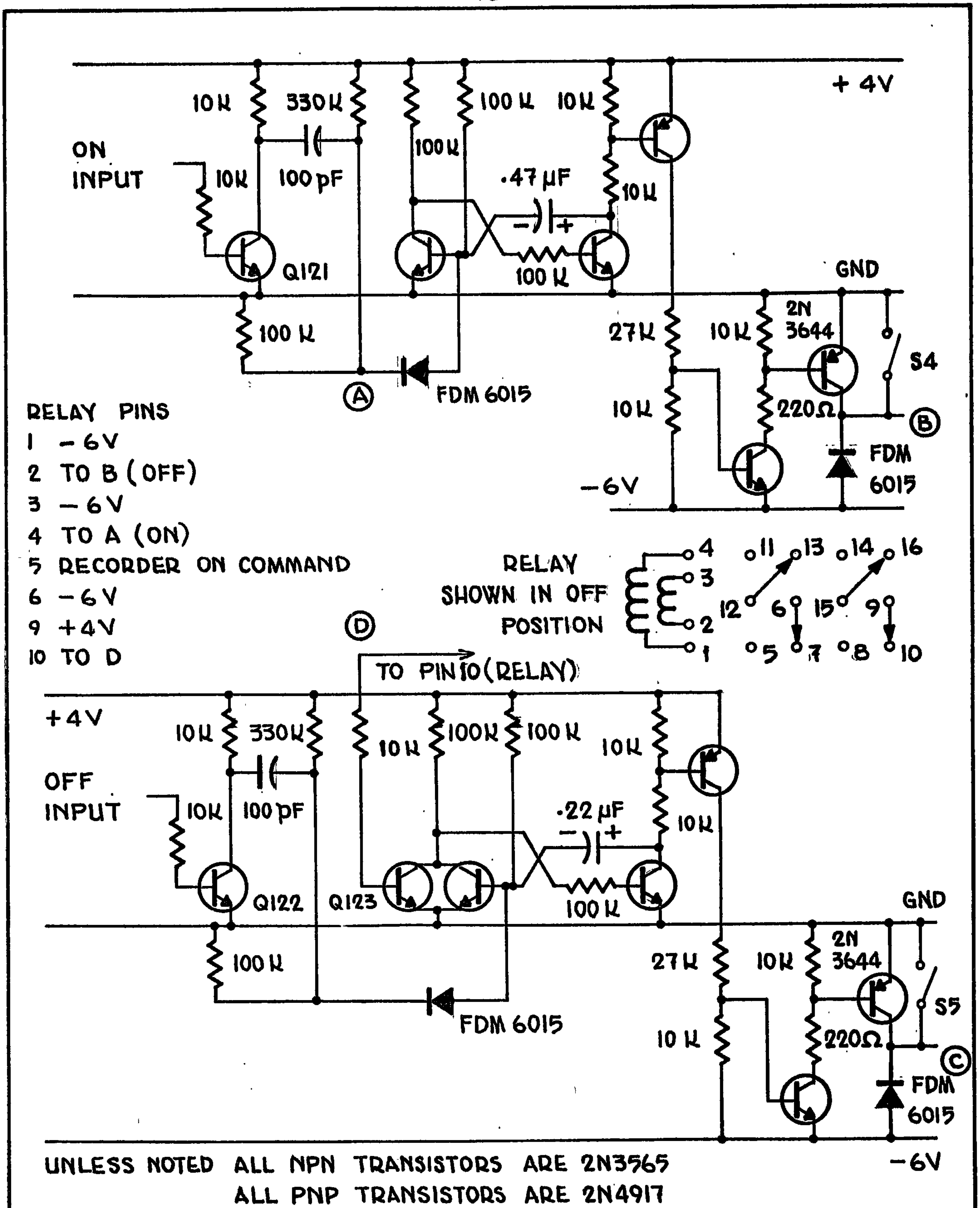


FIGURE 12 | SWITCHING | JULY 1968 W. G. M.

position the base of Q_{123} is held positive so that the one-shot is inhibited from firing.

Since the one-shots are triggered by a dynamic level change in their input lines, the buffers Q_{121} and Q_{122} are added to prevent level changes, due to loading the clock outputs, from switching the recorder. If the clock outputs are loaded by turning on the readout, more current is drawn from the buffers and the voltage output drops due to the current limiting effect of the load resistor (see Appendix 1). This will be seen by the relay one-shots as a dynamic level change and the relay will be switched. Hence the need for the buffers.

CHAPTER 4

PLAYBACK SYSTEM

4.1 Introduction

The playback system contains the various amplifiers and demodulators necessary to convert the F.M. information on tape into the original seismic signal and timing information. A block diagram of the playback system is shown in Figure 13. An external oscillograph-type recorder is used to obtain a visual record of the signals. If desired, a filter can be inserted between the playback panel and the oscillograph to enhance the signal by band-pass filtering. The unit is designed for use in the lab, where power is no longer a limiting factor. Wide use has been made of integrated circuits, which dictate the power supply voltages of +12 Volts and -6 Volts.

The information output consists of two signal channels and a time channel. A demodulator is required for each of these and one to demodulate the reference frequency to obtain the reference voltage, Vref.

Since the F.M. carrier is well within the audible range, it is easy for the human ear to detect the low frequency seismic signals as changes in the frequency of the carrier. It is thus possible to monitor the F.M. carrier of the information channels and detect the arrival of seismic energy before making visual records. An audio

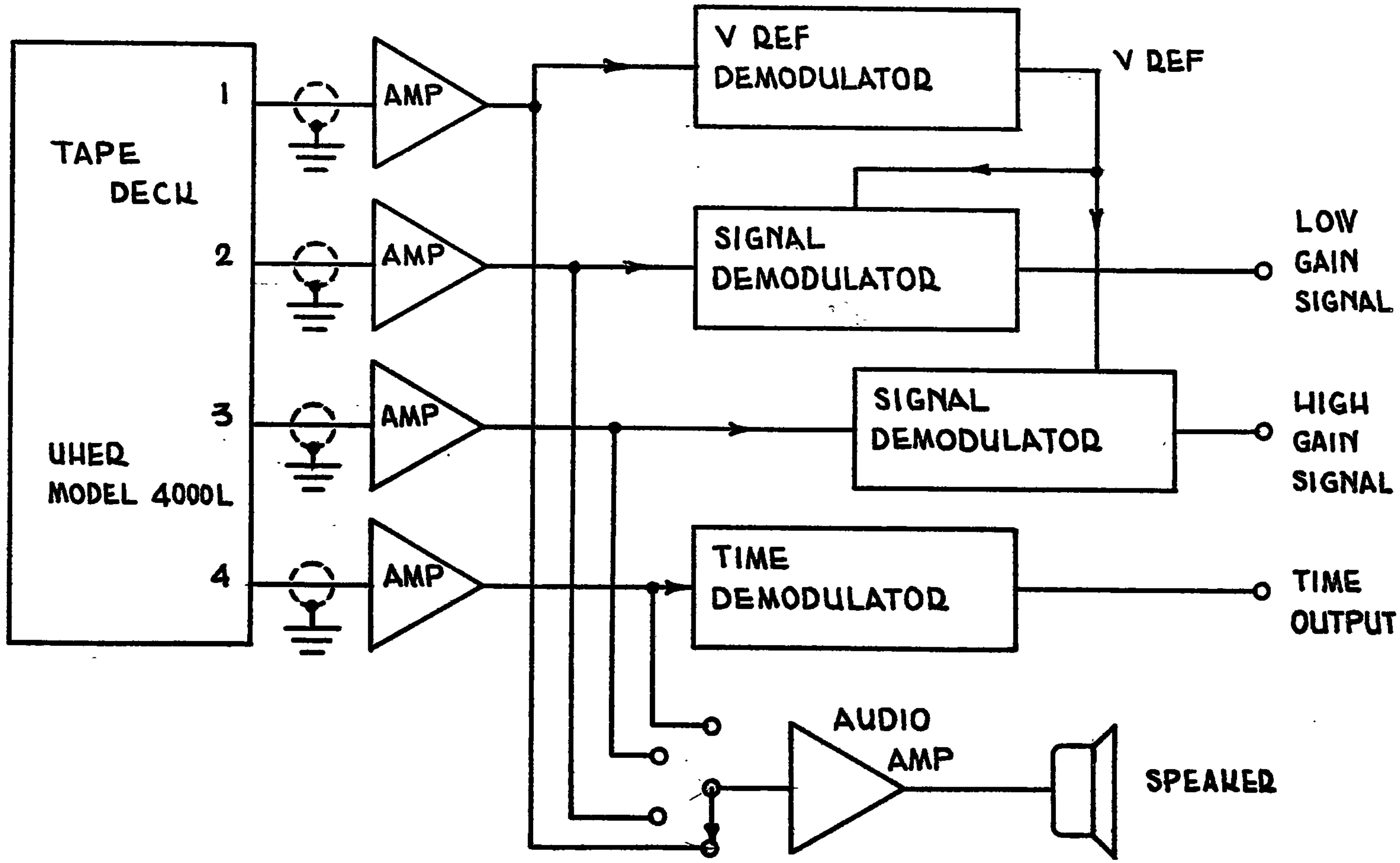


FIGURE 13 PLAYBACK BLOCK DIAGRAM

JULY 1968
W. G. M.

amplifier and speaker are provided for this purpose.

4.2 Functional Description of Units

The demodulators used to demodulate the time, signal and reference voltage are all of the pulse counting type, described in Section 2.2, and differ mainly in the method of forming the pulses. A block diagram of each is shown in Figure 14.

Each demodulator consists of an amplifier and Schmitt trigger to convert the signal from the tape into square pulses, a unit to shape these pulses and a filter to average the resulting waveform and remove the carrier.

4.21 Time Demodulator - The time demodulator is the simplest of the three. Only two frequencies are available at the input (720 Hz and 1440 Hz) and two voltage levels are required at the output. The input signal is shaped into rectangular pulses by the Schmitt trigger and switched between a constant voltage (-6 V) and ground. The switch remains on for the same length of time (.2 msec) for either frequency input. Thus the resulting pulses are all of the same width. However, for the higher frequency input the voltage is negative twice as often and the output level is greater after averaging than for the lower frequency.

4.22 Vref Demodulator - As was described in Section 2.2 the reference voltage Vref must be inversely proportional to the reference frequency input. This is provided in the Vref demodulator by charging a capacitor with a constant

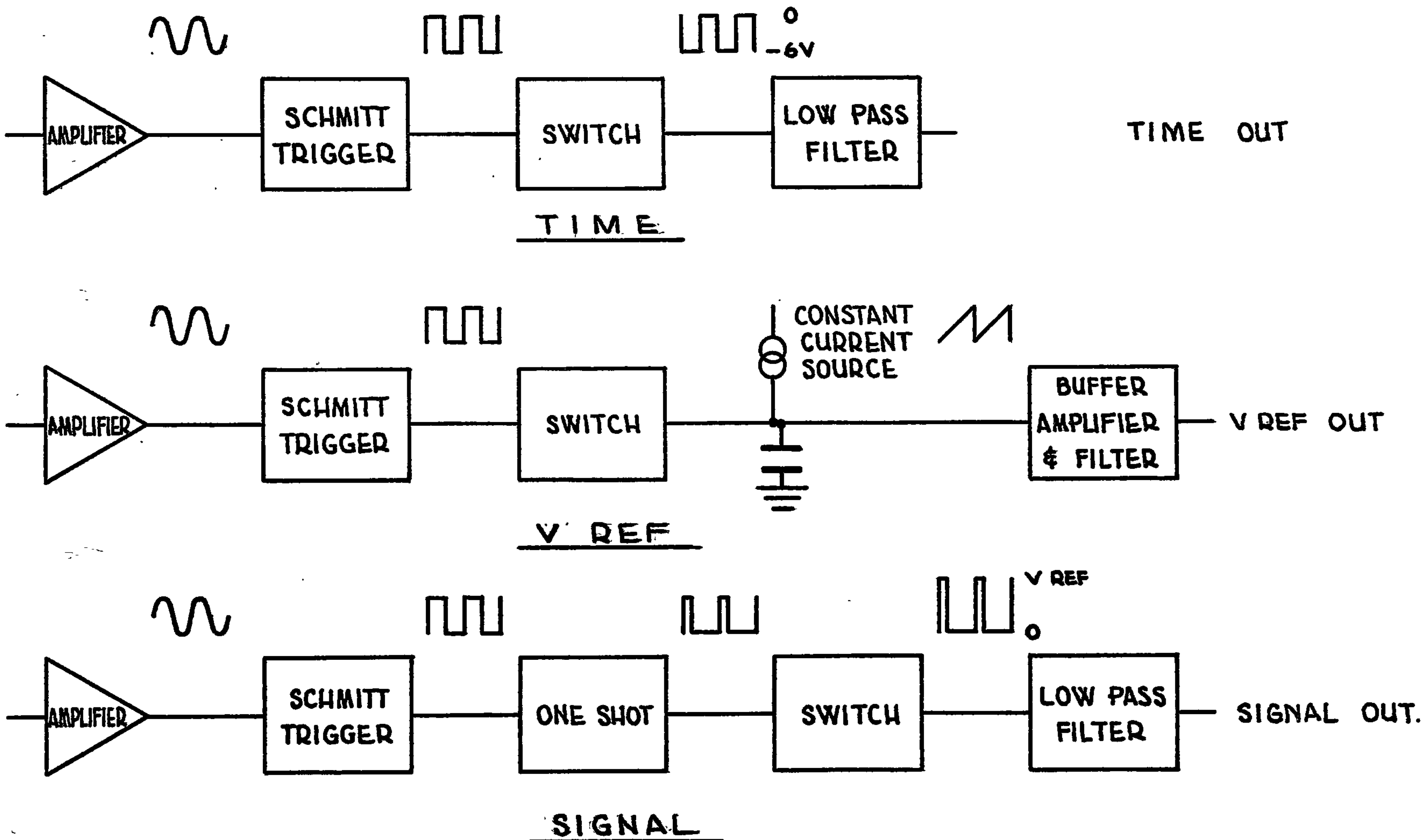


FIGURE 14 | PLAYBACK COMPONENTS | JULY 1968 WGM current during each period of the input signal and rapidly discharging it at the end of each cycle. Since the current is constant, the voltage on the capacitor is a ramp function. The lower the input frequency and hence the greater the period, the greater the voltage the ramp function is allowed to attain. After averaging, this appears as a higher voltage at the output.

4.23 Signal Demodulator - The signal demodulator is similar to the time demodulator, except that the tolerances are more stringent. It is in this unit that the accuracy of the playback lies and it must be assured that the output is a linear function of the input frequency. The addition of a one-shot assures that all the pulses entering the switch are of constant width and the signal output depends only on the input signal frequency. Following the method described in Section 2.2 on compensation, the pulses are switched between ground and the reference voltage, Vref.

4.3 Circuit Description

4.31 Pre-amplifiers - The low noise pre-amplifier shown in Figure 15 is used to provide enough voltage to drive the various demodulators. The signal available on playback from tape is in the order of 1 to 3 mV (see Figure 6). The gain of the low noise transistor stage Q_{151} is:

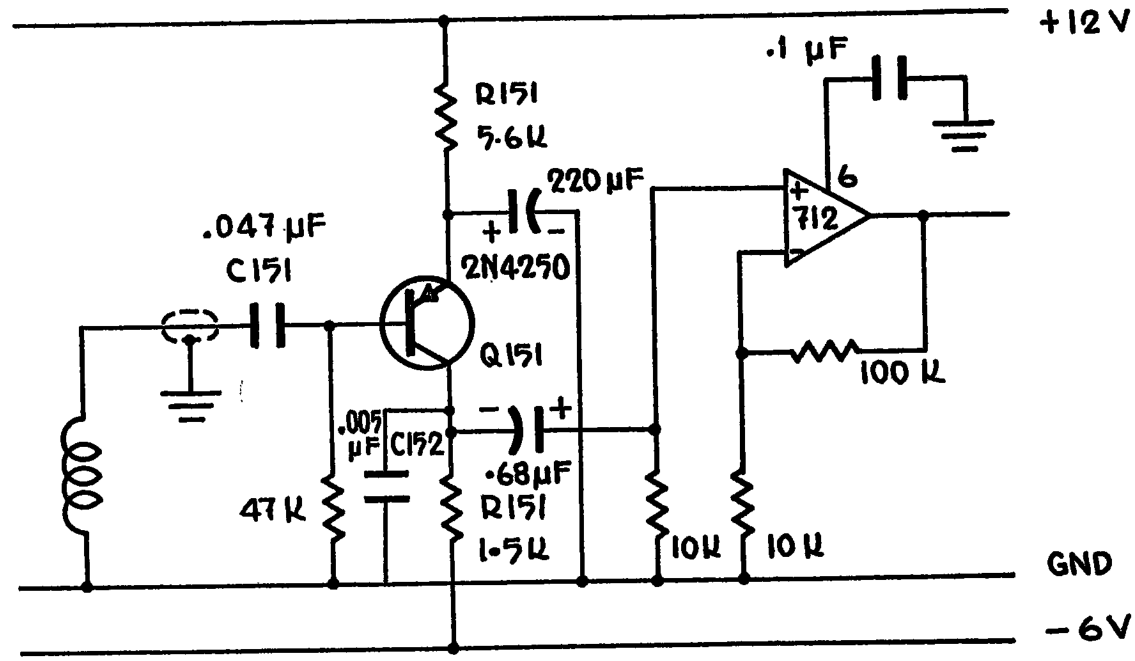


FIGURE 15 | PLAYBACK PREAMPLIFIER | JULY 1968 W. G. M.

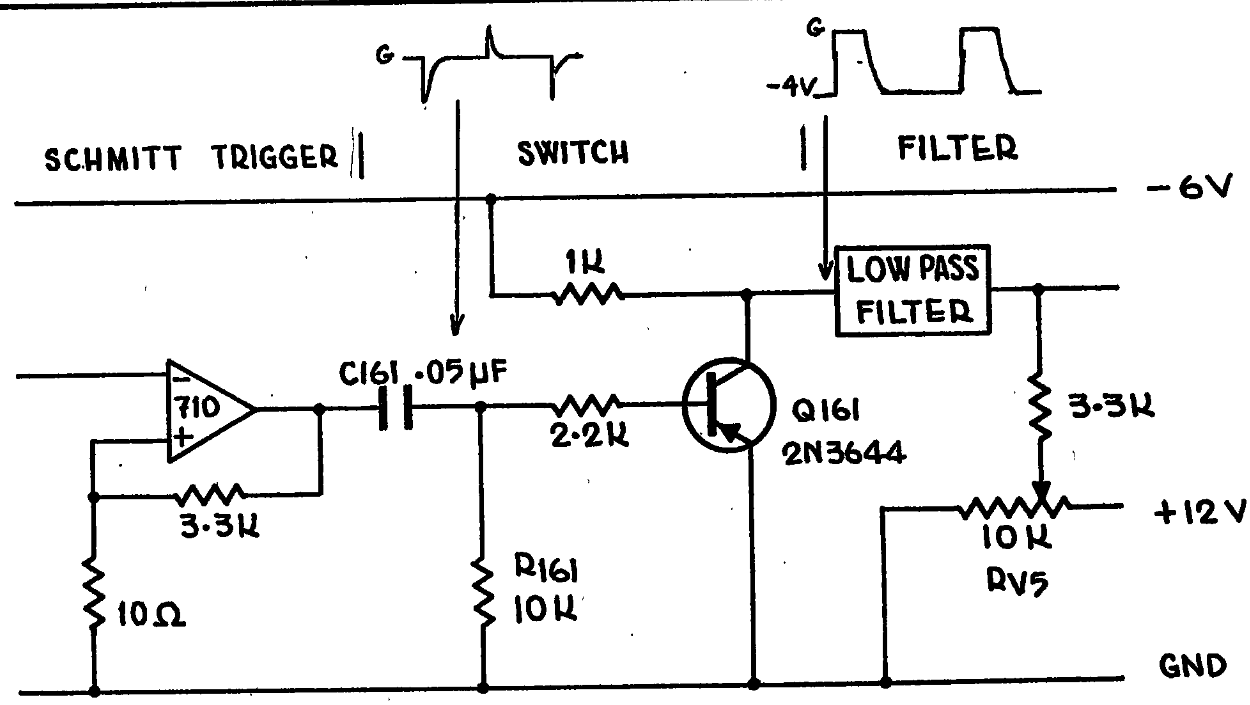


FIGURE 16 | TIME DEMODULATOR | JULY 1968 W. G. M.

$$A = \frac{V_{out}}{V_{in}} = \frac{R_L I_c}{V_{in}}$$

$$\text{where } V_{in} = h_{ie} i_b + h_{re} V_{CE}$$

$$= h_{ie} i_b = h_{ie} \frac{i_c}{\beta}$$

$$= .023 \text{ V. for most silicon transistors}$$

$$\text{and } I_C = \frac{12V + 6V}{R_{151} + R_{152}} = \frac{18V}{7.1K} = 2.5mA$$

$$\therefore \quad A = \frac{(1.5K)(2.5mA)}{.023 \text{ V}} = 163$$

The μA712 amplifier stage has a gain of 10 to give a total amplification of greater than 1500, providing from 1.5 to 4.5 V to drive the demodulators.

Since any DC current passing through the tape heads would set up an erase field, the capacitor C_{151} is used to block leakage current from the base of Q_{151}. It also acts as a high pass filter, with a 3 db point of 60 Hz. A high frequency cut-off to prevent the amplifier from oscillating is provided by the capacitor C_{152} in parallel with R_{152} for a 3 db point at 20 KHz. The cut-off is placed far enough above the frequency range of interest that the phase shift is linear over this range.

4.32 Schmitt Trigger - The first stage of all three types of demodulators is a Schmitt trigger. It is used as a squaring circuit to convert the AC signal on the tape into pulses suitable for triggering the demodulators. The circuit is as shown below:

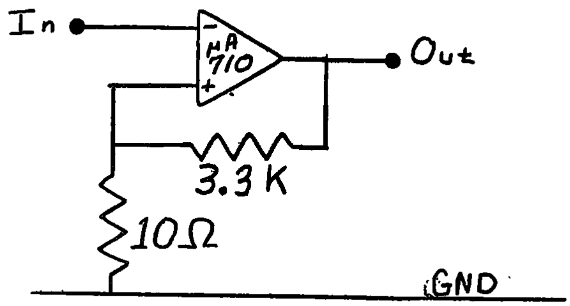


Figure 17. Schmitt Trigger

Feedback is used to provide a certain amount of hysteresis which prevents the unit triggering on input signal noise and speeds up the rise and fall times by assuring that the output is in saturation at all times. The μA710 is a dual input voltage comparator with output voltage levels of -.5V and +3.2V. The feedback network of 3.3K and 10 ohms provides a voltage at the positive input of

$$\frac{10}{3.3K}(-.5V) = -1.5mV$$

in the off state, and

$$\frac{10}{3.3K}(3.2V) = 10mV$$

in the on state. The unit will trigger when the input voltage reaches these levels and the following hysteresis loop is achieved:

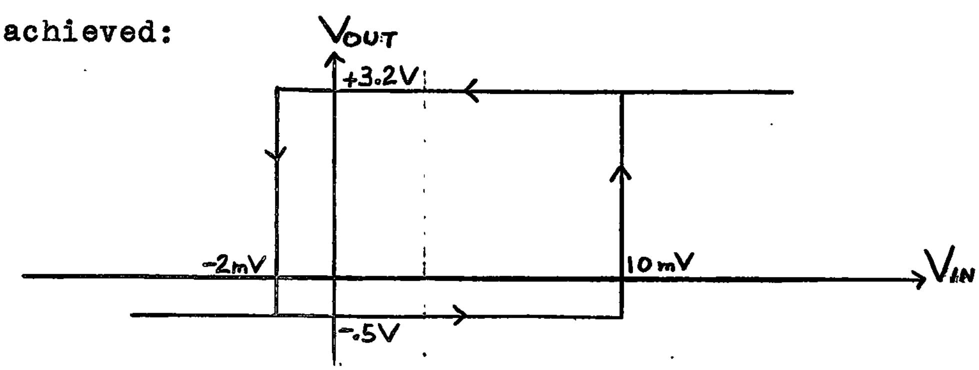


Figure 18. Schmitt Trigger Response

4.33 <u>Filters</u> - The last stage of each demodulator is a low pass filter which averages the pulses and removes the carrier frequency. The filter is a passive RLC type manufactured by Data Control Systems (DCS). It has a 3 db point of 200 Hz and a high frequency roll-off of 30 db/octave.

4.34 <u>Time Demodulator</u> - The time demodulator is shown in Figure 16. After passing through the amplifier and Schmitt trigger, the FM time signal, by this time a rectangular wave train of amplitude 3.2 V, is differentiated by the capacitor-resistor combination $R_{161}C_{161}$. The time constant of this pair is such that Q_{161} remains on for .2 msec. following the start of each cycle of the input frequency. This "on time" of the switch is less than the period (.7 msec) of the higher of the two frequency inputs (1440 Hz). The waveform entering the filter is nominally at approximately -4 Volts and is pulsed to ground for .2 msec at a rate of either 720 or 1440 Hz. The output after filtering will be the average over one period, or:

$$V \times \frac{t_2 - t_1}{t_2} = -4V \times \frac{.5\text{msec}}{.7\text{msec}}$$

$$= -2.8 \text{ Volts}$$

where t_1 = switch "on-time"

t_2 = one period

for the higher frequency and in the same way -3.4 V for the lower frequency. To make it easy to record on a DC recorder, the DC level of the less negative voltage is returned to ground by a DC offset through Rv_5. This gives output levels for the two states of 0 and -.6 Volts.

4.35 Vref Demodulator - As was described in Section 4.22 the .5μf capacitor C_{192}, in Figure 19, is charged by a constant current source (to be described below). The input to this demodulator is the reference frequency and is nominally constant at 720 Hz or 1.4 msec period. The demodulator output, Vref, is set at 5V for a 720 Hz input. The current required to charge the capacitor is therefore:

$$I = \frac{CV}{T} = \frac{.5\mu f \times 5V}{1.4 msec} = 1.8 \text{ mA}.$$

As in the time demodulator, the square wave from the Schmitt trigger is differentiated by the $R_{191}C_{191}$ combination. The switch, Q_{191} and Q_{192}, is on for approximately 150 usec at the start of each cycle of Fref. The purpose of this switch is now to discharge the capacitor C_{192}. Since it must handle a current of

$$I = \frac{CV}{T} = \frac{.5\mu f \times 5V}{150\ \mu sec} = 65 \text{ mA}$$

the two stages Q_{191} and Q_{192} are needed.

It is desired that all the current from the constant

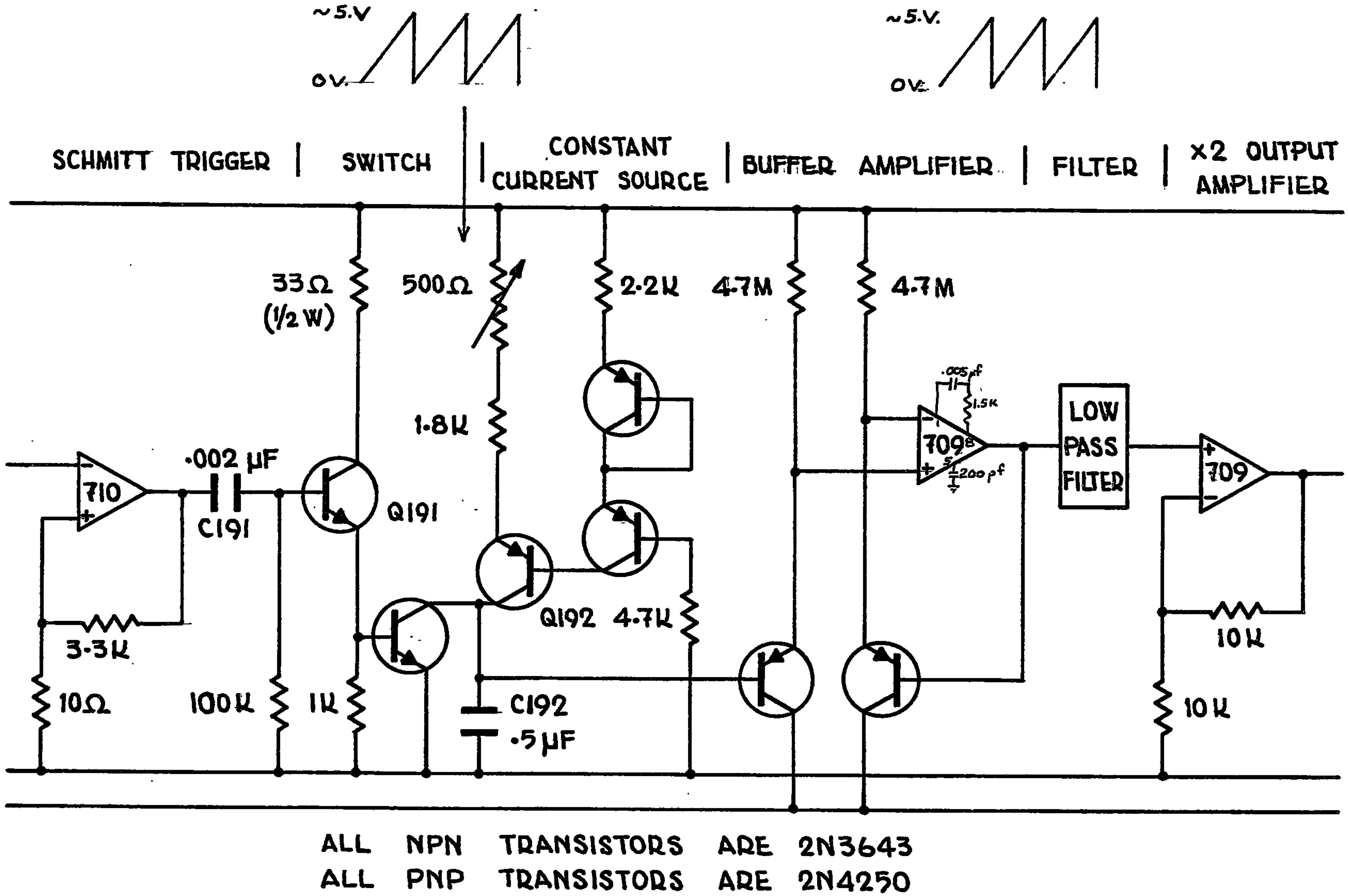


FIGURE 19	V REF DEMODULATOR	JULY 1968 W. G. M.

current source be used to charge the capacitor and not to drive the next stage. The high input impedence buffer draws only in the order of

$$i_B = \frac{18V}{(R_L)(\beta)} = \frac{18V}{4.7M \times 300} = 15 \text{ nA}$$

which, even including the base leakage current, is negligible compared with the charging current of 1.8 mA. The buffer has unity gain and the signal entering the filter is equal to the ramp function on the capacitor. The average value of the ramp function after filtering is

$$\tfrac{1}{2} \text{ Vmax} = 2.5 \text{ Volts}$$

and the final output amplifier has a gain of 2 to give a nominal output voltage of 5 Volts for Fref = 720 Hz.

The <u>Constant current source</u> used in the Vref demodulator is shown below.

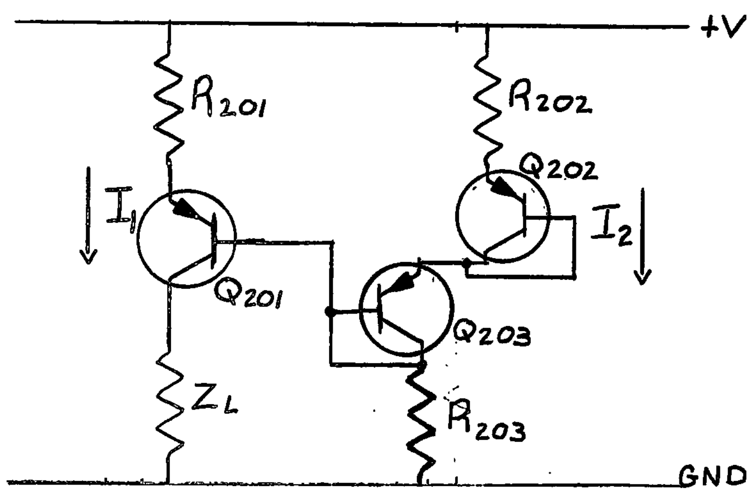


Figure 20. Constant Current Source

The transistors Q_{201} and Q_{202} are held in the on state by having their bases attached to the collectors and the current I_2, neglecting the base currents, is

$$\frac{12V - 2V_{BE}}{R_{202} + R_{203}} = \frac{12V - 1.2V}{4.7K + 2.2K} = \frac{10.8V}{6.9K} = 1.57 \text{ mA}$$

where V_{BE} = base-emitter saturation voltage = -.6V

This current holds the collector of Q_{203} and the bases of Q_{201} and Q_{203} at a voltage of

$$I_2 \times R_{203} = 1.57 \text{ mA} \times 4.7K = 7.4 \text{ V}$$

and the emitter of Q_{201} at

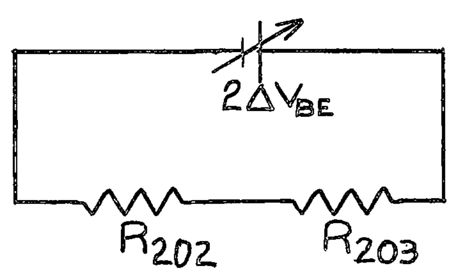
$$7.4V - V_{BE} = 8.0 \text{ V.}$$

Since the voltage drop across R_{201} is defined at

$$12 - 8V = 4 \text{ Volts}$$

the current I_1 can be adjusted by varying R_{201}, and is independent of the load, Z_L. For the present application a current of 1.8 mA. is required and $R_{201} = \frac{4V}{1.8mA} = 2.22K$

The second transistor Q_{202} is added for temperature compensation. The base-emitter voltage has a temperature coefficient of -2.3 mV/C°. Considering only the voltage changes induced by the temperature variations of Q_{202} and Q_{203} the 12V power supply can be considered as an ac short circuit so that:



where the temperature variation in V_{BE} of Q_2 and Q_3 is considered as a variable voltage 2 V_{BE}. The voltage change across R_{203} (ΔVR_{203}) is then

$$\frac{R_{203}}{R_{202} + R_{203}} \times 2\Delta V_{BE} = \frac{4.7K}{4.7K + 2.2K} \times 2(-2.3mV) = -3.1mV/C°$$

Since the voltage across R_{201} is held at 4 Volts this variation is

$$\frac{-.8mV/C^{o}}{4\ V} = -200ppm/C^{o}$$

and the "constant" current has the same temperature coefficient. The capacitor C_{192} has a temperature coefficient of -130 ± 30 ppm/C° and the decrease in capacitance will be offset by the corresponding drop in charging current. The total error in the voltage is

$$-(-130ppm/C^{o} - (-200ppm/C^{o})) = -70ppm/C^{o}$$

A similar analysis shows that if Q_{202} is omitted the error is+350 ppm/C°.

4.36 Signal Demodulator - The first stages of the signal demodulator, shown in Figure 22, are similar to those of the time demodulator except for the addition of a one-shot.

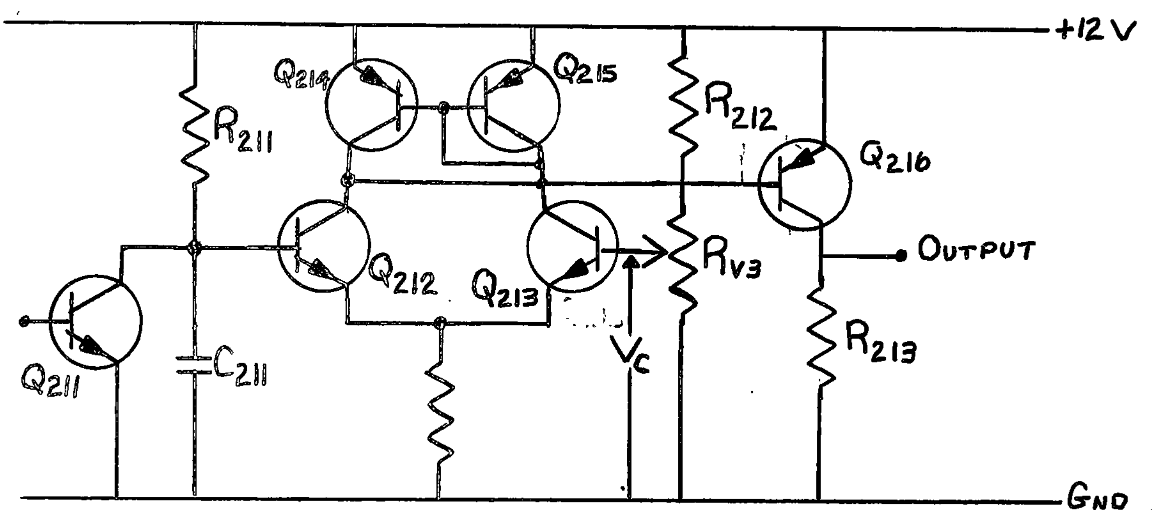


Figure 21. One Shot

The one shot shown above is basically the differential amplifier described in Section 2.33 with one input, Q_{213}, held at a constant voltage, V_c, and the other input, Q_{212},

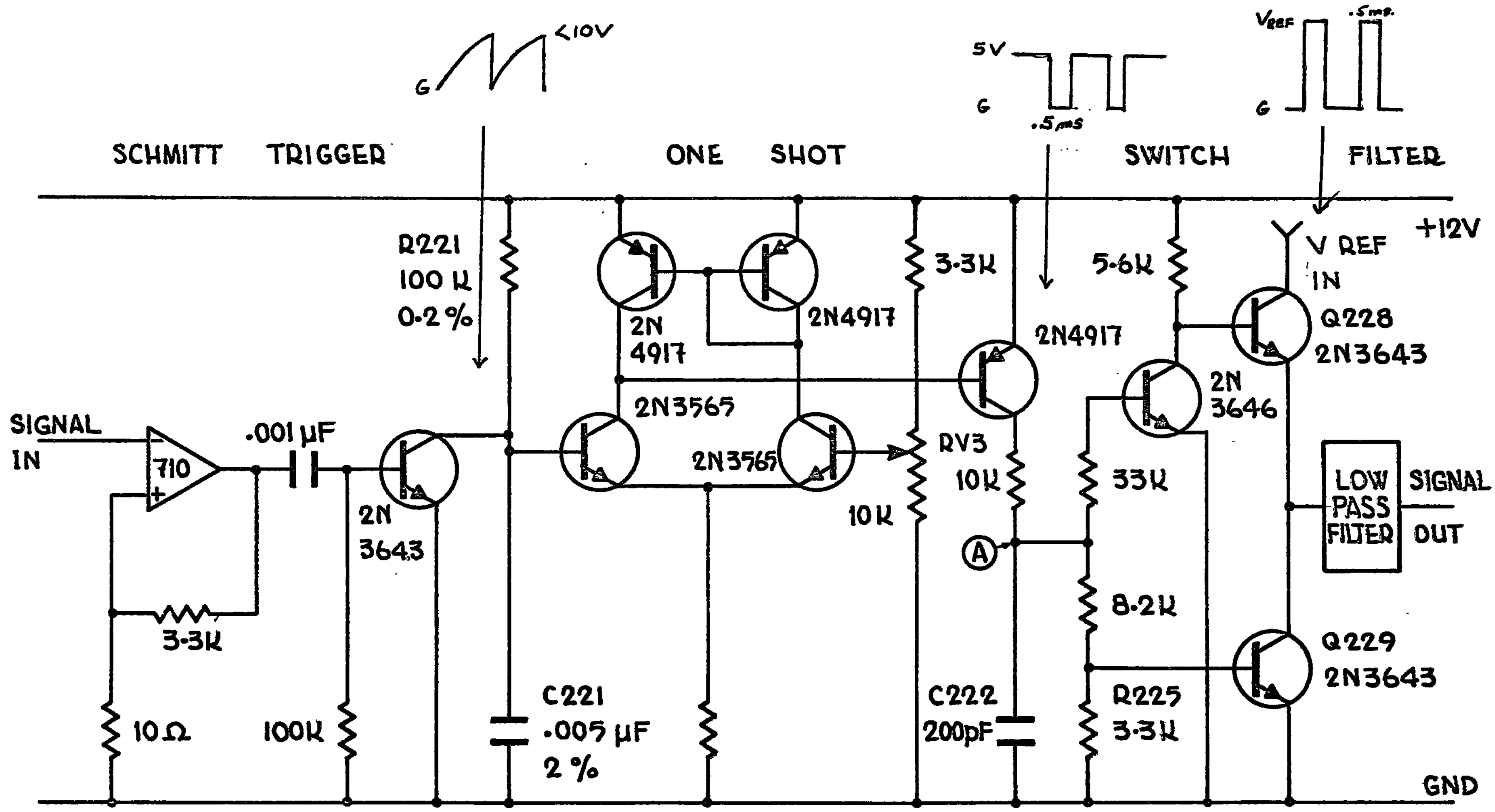


FIGURE 22 | SIGNAL DEMODULATOR | JULY 1968 | W.G.M.

connected to a charging capacitor, C_{211}. The capacitor is discharged by the switch, Q_{211}, at the start of every cycle of the input signal. It is then charged through the resistor, R_{211}. When the voltage on the capacitor reaches V_c the transistors Q_{212} and Q_{216} turn on and the output rises from ground to +12V.

The output is a +12V pulse, the width of which is determined by the time necessary for the voltage at the base of Q_{212} to reach V_c. The record modulator is linear up to 1500 Hz, so that the highest frequency into the demodulator will be 1500 Hz or .67 msec period. If the on time of the one-shot is set just below this at .5 msec the voltage V_c must be equal to the value the capacitor reaches in that time, or:

$$
\begin{aligned}
V_c &= 12V(1 - e^{-\frac{T}{RC}} \\
&= 12V(1 - e^{-\frac{.5msec}{.5msec}}) \\
&= 12V(1 - .37) \\
&= 7.6 \text{ Volts}
\end{aligned}
$$

and the resistance from the base of Q_{213} to ground must be approximately:

$$
\begin{aligned}
R &= \frac{7.6V}{12V} (R_{213} + R_{214}) \\
&= \frac{7.6V}{12V} (10K + 3.3K) \\
&= 8.5K
\end{aligned}
$$

The 10K variable resistor Rv_3 is used to adjust this value and set the width of the pulses.

The final stage of the demodulator switches the output of the one-shot between Vref and ground. To assure that the filter feeds from the same source impedence when the switch is in either the on or off state, the two transistors Q_{228} and Q_{229} are used. The filter then sees the saturated collector-emitter resistance of the relevant "on" transistor for either state. The capacitor C_{222} and pull-down resistor R_{225} are arranged to slow down the one-shot output pulse on the base of Q_{229} so that it cannot turn on while Q_{227} and Q_{228} are still on.

The output of the demodulator is:

$$V_{out} = V_{ref} \frac{T_{on}}{T_p}$$

$$= V_{ref} \, T_{on} f_s$$

where T_{on} is the constant on time of the one-shot,

and T_p is the time of one period of the input signal, f_s

and the output varies directly as the frequency and the reference voltage.

4.37 <u>Audio Amplifier</u> - The audio amplifier shown in Figure 23 is used to monitor the FM signals on playback as mentioned in Section 4.1.

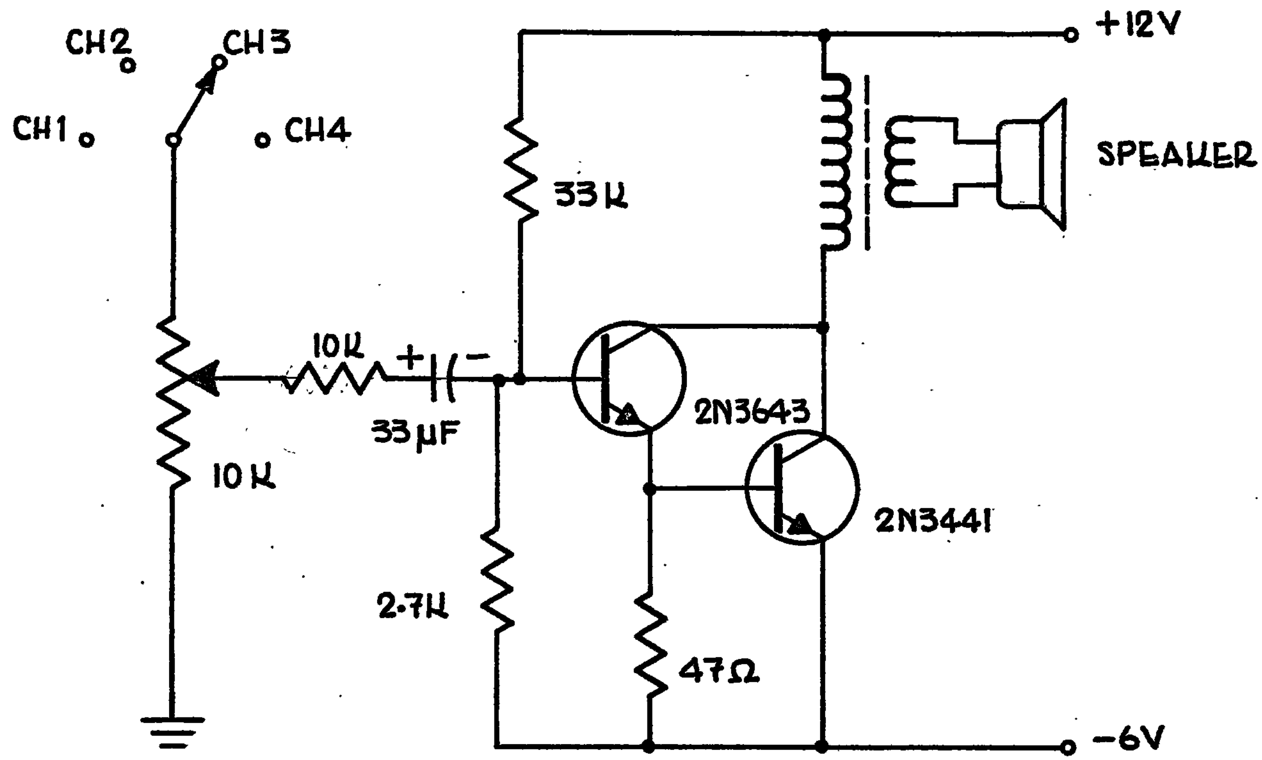


FIGURE 23 | AUDIO AMPLIFIER | JULY 1968 W.G.M.

CHAPTER 5

PERFORMANCE

5.1 Sea Trials

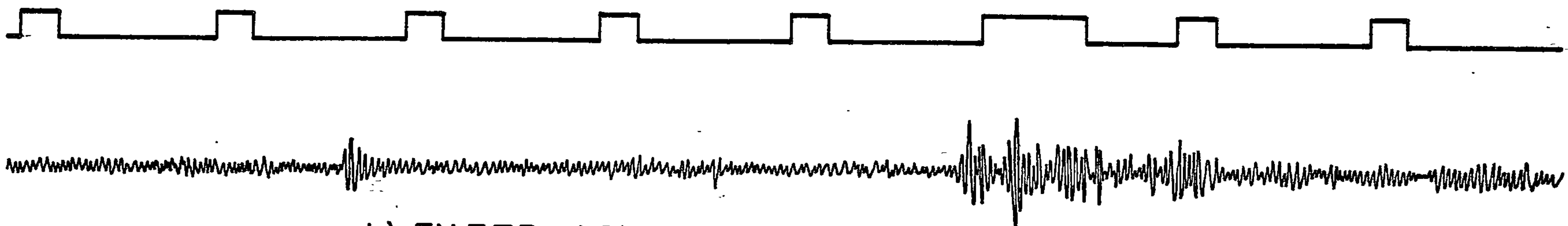
During the month of July, 1968, on Phase III of Bedford Institute Cruise 22-68, the complete system was tested as part of the preparation for a refraction experiment to be carried out by C.E. Keen on Phase IV of the cruise.

The recorders were used with the Dalhousie sonobuoy hydrophones mentioned in Section 2.31 and were placed in the buoys used for the Bedford Institute radar transponders. The recording buoys were placed in the water on two occasions for up to three hours. They were allowed to drift freely and recorded signals, using a 10 cubic inch Bolt Air Gun, towed from the CSS HUDSON, as an energy source.

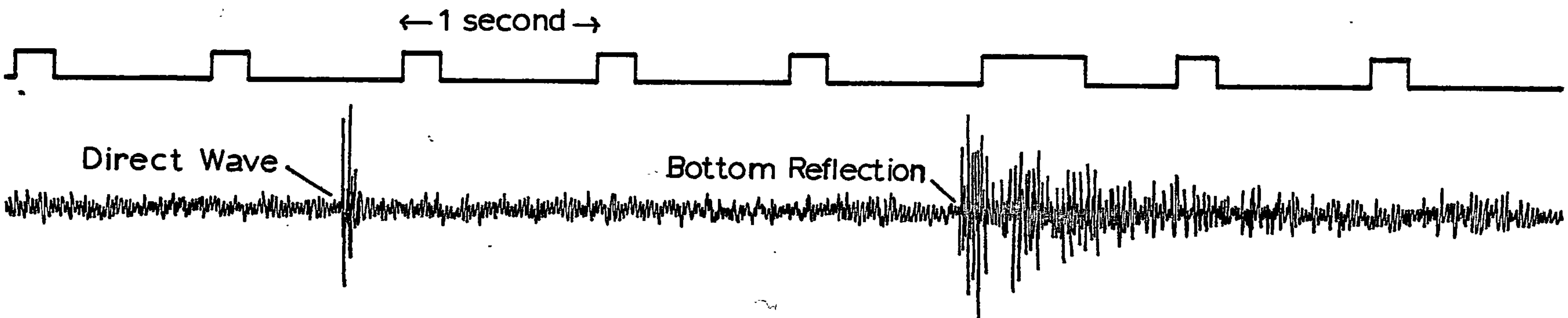
On the first test the recorder was programmed to turn on every four minutes for two minutes. The Air Gun was triggered every twelve seconds during three of the periods in which the system was recording. The distance between the buoy and the Air Gun varied from 1.5 miles to .1 miles during this time. Good arrivals were apparent for all firings of the Air Gun.

Figure 24 shows both direct and bottom reflected arrivals for one of these shots, using three different playback filter settings. These records were made using an ultra-violet

a) FILTER: LOW CUT OUT, HIGH CUT 100 Hz.



b) FILTER: LOW CUT 4 Hz., HIGH CUT 40 Hz.



c) FILTER: LOW CUT 4 Hz., HIGH CUT OUT

FIGURE 24 AIR GUN RECORD

galvanometer recorder and a Kron-Hite variable filter. The separation between the recorder and Air Gun was approximately .2 nautical miles and the water depth was about 1500 fathoms. The HUDSON was towing the Air Gun at 3 Knots. The low frequency noise in Figure 24a was caused by wave motion in the hydrophone suspension and was removed, as described in Section 2.32, for the second test. For reasons to be discussed below the flutter compensation voltage, Vref, was not used in making the records in Figure 24.

During the second test the recorder was programmed to turn on for one minute every ten minutes. The Air Gun was again towed from the HUDSON, but this time at higher speeds and did not approach as close to the buoy. The arrivals were again apparent but not as obvious as those in Figure 24. This was due mainly to the fact that the Air Gun is not as efficient when towed at high speeds because of water turbulence from the ship. The amplifiers had been modified as described in Section 2.32 and the low frequency noise of Figure 24a was not observed.

5.2 Component Performance

A brief summary of the system is shown in Table 3. Time has not permitted extensive testing of many of the components of the system. All of the units have performed satisfactorily and the general characteristics are known. Future tests must be made to determine the exact temperature performance, accuracy and dynamic range.

5.21 Amplifiers and Modulators - The nexus Q-200 low-power amplifiers have been very satisfactory. Preliminary tests indicate that their low frequency noise figure is very good (less than 10 db at 10 Hz). The modulator response is shown in Figure 25. Tests on the initial design model (Fitzgerald, 1967) indicated a linearity of .1% and a temperature coefficient of 300 ppm/°C.

Information	4 Channels	1 reference frequency 2 low gain seismic 3 high gain seismic 4 time code
Amplifiers	Passband Gain	4 - 150 Hz two channels separated by 30 db Low gain -10 to +40 db High gain +20 to +70 db
Modulators	Center freq. Deviation	750 Hz ±250 Hz for -.7 to -1.4V input
Dynamic Range	greater than 70 db apparent range using both gain channels	
Clock	Cycle Stability	24 hours better than 1 ppm/°C
Timing	pulses each second, with 6 sec. and 1 min. identification and an hour code on each record	
Switching	Interval and duration of records adjustable in BCD steps from .8 min. to 2 hr.	
Tape Recorder	Uher 4000L Heads Recording time	15/16 ips Nortronics 4 channel 180 min. active recording on mil. tape
Power Consumption	Clock and switching Amplifiers and Modulators Tape Recorder	1.2 W. 2 mW. 2.1 W., when active

TABLE 3. SYSTEM DESCRIPTION

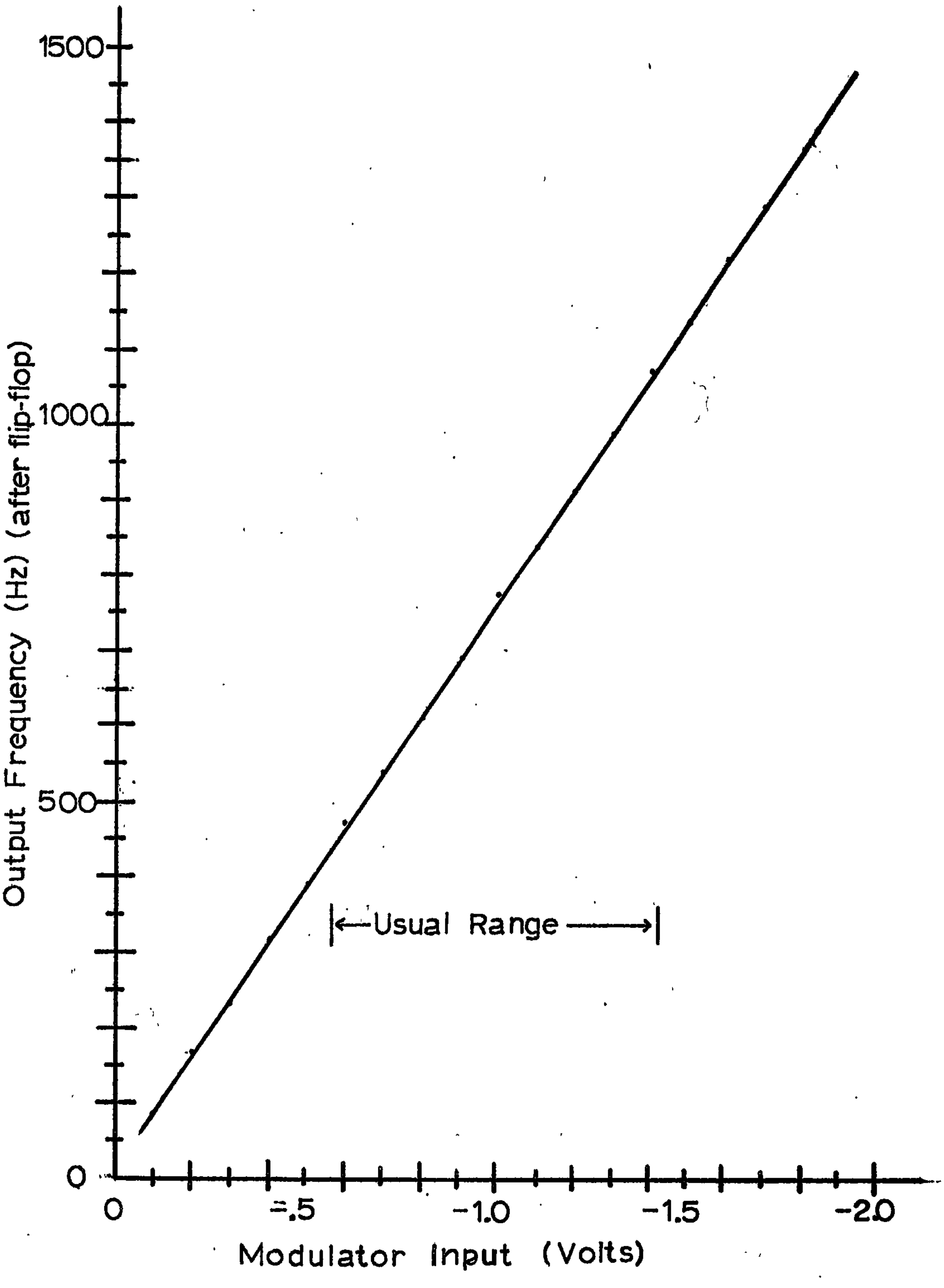


FIGURE 25 MODULATOR RESPONSE

5.22 Tape Recorder - It was feared that the speed of the Uher recorders would be affected by the severe motion of the buoy in a heavy sea. It was mainly for this reason that the reference frequency compensation channel was developed. The tests carried out at sea indicate that the effect is not as severe as suspected. The records of Figure 24 were made without the flutter correction and, although the seas were moderately high when the shot was recorded, the expected noise is not apparent. On playback there is not an audible change in the frequency of the reference channel.

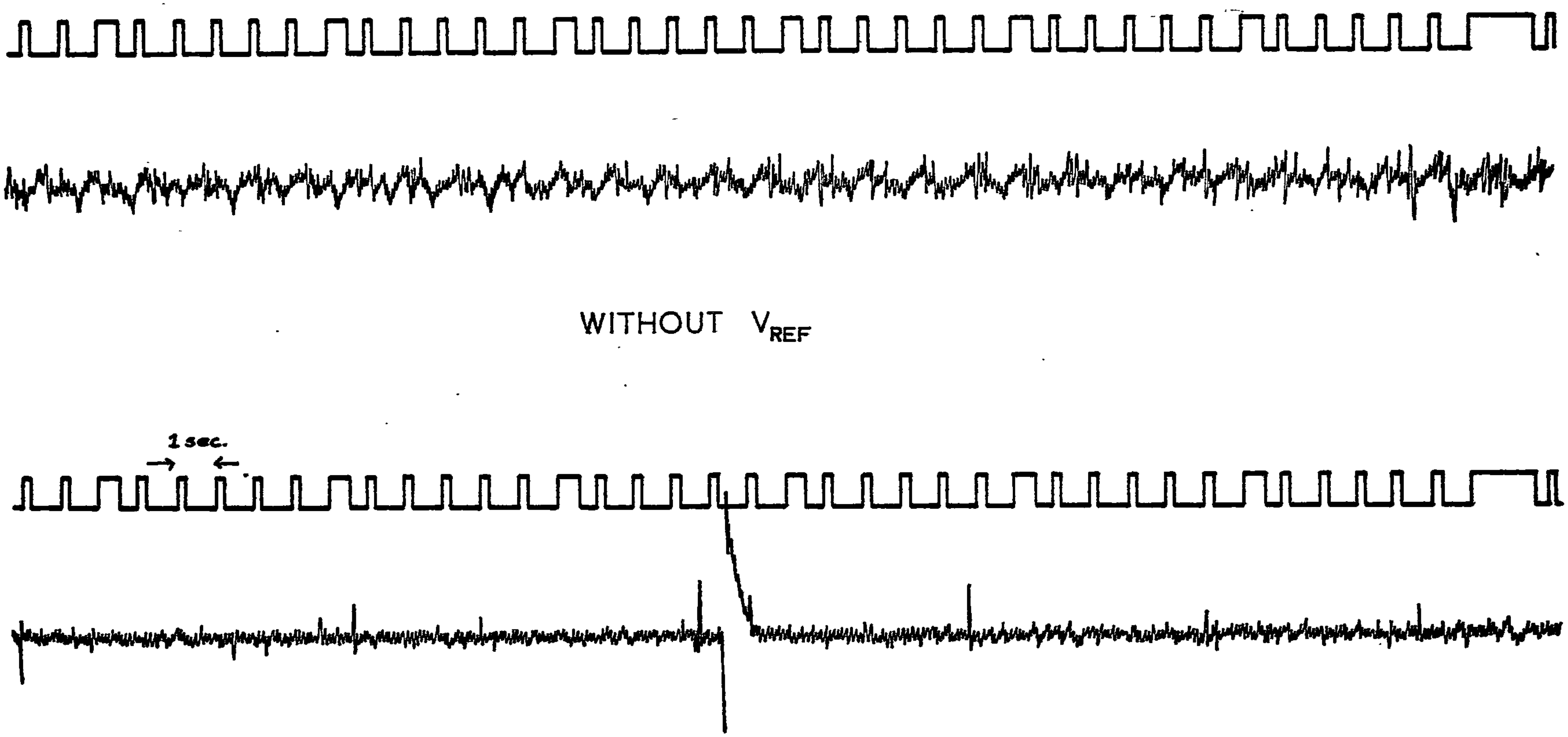
5.23 Clock and Switching - The original manufacturer's specification for the stability of the oscillator was .05 ppm/°C. This was not achieved and was revised to 1 ppm/°C. Two lots of crystals were received. One of the first group was tested in the laboratory and showed a stability of .7 ppm/°C, from 02 to +20°C. The second set was tested by the manufacturer before shipping and the stability ranged from .2 to .8 ppm/°C, over the range 0 to 15°C.

If the temperature variations are considered periodic (diurnal) and the long term drift assumed linear over the time the recorder is operating, this stability should prove satisfactory for experiments of short duration. It would be interesting to determine the exact temperature variations in a buoy on the sea surface. If the life of the recorder is to be extended beyond four or five days, a more constant temperature environment, as mentioned in Section 3.21, must be provided, or a more stable crystal used.

5.24 Playback.- The only serious problem encountered has been with the flutter correction system. Figure 26 shows two playbacks of a zero input record made in the laboratory. Figure 26a shows some cyclic noise that appears to be associated with the mechanical drive of the Uher recorder. As Figure 26b (same scale) shows, the compensation does remove much of this noise, but introduces numerous spikes. These are caused by drop-outs on the magnetic tape or dust particles, causing a break in the reference frequency. They cause large amplitude noise if the Vref voltage is used in playback. It is necessary to lower the cut off frequency of the averaging filter of the Vref demodulator (at present 200 Hz) to approximately 10 Hz, so that high frequency spikes are not passed. Care must be taken to ensure that phase shift is not introduced between the compensation and signal channels. This can be done by designing a zero phase shift filter for the Vref demodulator or shifting the signal channel by the same amount as the Vref channel. An alternate method would be to design a phase lock loop that would detect and bypass any sudden changes in the Vref output.

5.3 Conclusion

The initial stages of developing and testing this system have now been completed. It is hoped that the results of the refraction experiment being conducted on the Mid-Atlantic Ridge at the time of writing of this thesis, will prove the value of the system as a marine seismic recorder.



WITH V_{REF}

FIGURE 26 FLUTTER CORRECTION

There are a number of modifications that should be incorporated in the future. Some of these have been mentioned in the last section.

The life of the system could be greatly increased by lowering the power consumption of the clock, which at present constitutes the largest power drain. Development is continuing at the Bedford Institute on low power clock flip flops. It appears possible to reach a level of 50 microwatts or less, per flip flop, which would lower the power consumption of the clock by almost a factor of five hundred. The use of magnetic core storage elements, for the shift register in the time code circuit, would lower the power even more.

If the Fref and timing channels were combined on one tape channel, an extra seismic channel could be recorded. This could be for high frequency water wave information in marine use, or an additional velocity component on land or the ocean bottom. This is done in the Cambridge recording buoys (D. McKeowen, personal communication) and involves incorporating a delay in the reference frequency demodulator so that it does not see the doubling of the frequency in the time code.

It is doubtful whether it would be useful to place a system, such as this one, on the ocean bottom for refraction studies at sea. The information gained in the additional S wave arrivals, which are not transmitted through water, and the chance of improved signal-to-noise ratio, does not warrant the extreme problems involved in bottom placement and retrieval, especially considering the short length of time involved in most refraction experiments. It would be very worthwhile, however, to place a recorder on the bottom for long term studies of earthquakes and microseisms. It is hoped that future developments will involve the incorporation of this system in a bottom placement mechanism for such studies.

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APPENDIX I

LOGIC ELEMENTS

This appendix contains a description of flip flops, gates and buffers as logic elements. A detailed explanation of the circuit design and electrical characteristics of each type of circuit can be found in Millman and Taub (1965) Chapters 9 and 10 or the General Electric Transistor Manual (1964) Chapters 5 and 7. The circuits of the Motorola mwMRTL units used in the clock are discussed in Motorola Application Notes AN236, AN252, AN253.

Logic Levels - Binary logic circuits have only two stable states--either on or off. These states are usually indicated 1 and 0 respectively. Throughout this system, positive logic is used, the 1 state being more positive than the 0 or ground state. The inverse of a given state is designated by a superscripted bar--the inverse of 0 is $\overline{0}$ or 1, the inverse of A called "not A" is written $\overline{A}$, etc.

Of importance in the switching of logic elements is the transition from one state to the other. The transition from 1 state to the 0 state is called a dynamic zero and in positive logic is a negative going transition. Similarly, a dynamic one is the transition from the 0 state to the 1 state, or a positive going transition.

<u>OR, AND and NOT</u> - The two main operations in logic systems are those of OR and AND. These are best described in terms of black boxes with any number of inputs and one output.

In the OR operation, designated by

$$F = A + B + \ldots$$

the output (F) assumes the 1 state if any of the inputs is 1, and is 0 only if all the inputs are 0.

The output of an AND operation, designated by

$$F = A \cdot B \cdot \ldots$$

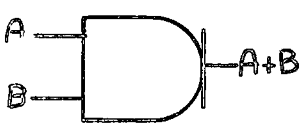
assumes the 1 state if and only if all the inputs are 1 and is 0 if any input is 0.

The NOT operation or inversion, designated by a superscripted bar, simply inverts the input. The output is 0 for an input in the 1 state and is 1 for an input in the 0 state.

These operations are described in the truth tables below. The symbols for the operational elements or gates are shown. The circle on the output of the NOT gate signifies inversion.

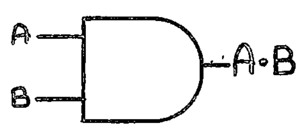
<u>OR</u>

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1



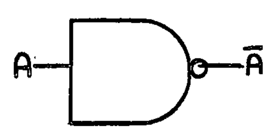
<u>AND</u>

A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1



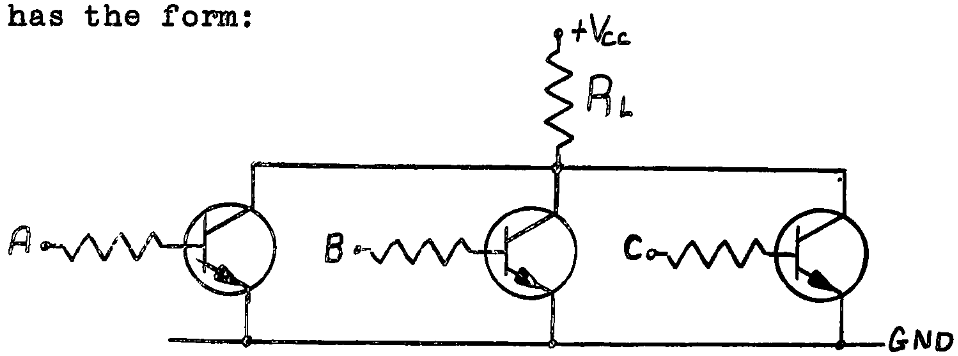
<u>NOT</u>

A	$\bar{A}$
0	1
1	0



The operations described above follow the rules of Boolian algebra which are reviewed in Millman and Taub (1965), Chapter 9.

Gates - The black boxes which perform the operations described above are called gates. In the RTL or resistor-transistor logic used in the Motorola mwMRTL series, the basic gate has the form:



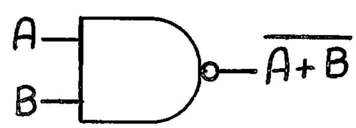
If all the inputs are at ground the transistors are all off, no current flows through R_L, and the output is at V_{cc}. If any one of the inputs is taken positive, that transistor turns on, acts as a short circuit, and the output drops to ground. The output is thus in the 1 state if all inputs are 0, and drops to the 0 state if any of the inputs is 1. This is the inverse of the OR operation and is called NOT OR or NOR. It is written

$$F = \overline{A + B}$$

This is essentially the only logic operation used in the present system and its truth table is summarized below for reference:

NOR

A	B	$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0



The Motorola mwMRTL units used are type MC817P which contains four 2-input gates and type MC819P which contains two 4-input gates.

Inverter - If all the inputs of a NOR gate except one are held at ground (0), the output is the inverse of the remaining input. In this manner the NOR gate can be used to perform the NOT or inversion function.

Inhibit - If one input of a NOR gate is held positive (1), the output will remain at ground (0) no matter what the other inputs are. In this manner the gate can be used to perform the inhibit function, preventing the output from changing even if the other inputs change state.

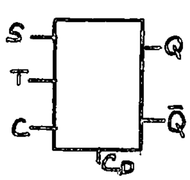
Buffer - As can be seen from the form of the basic gate, the output current is limited by the collector resistor R_L. This means that only a limited amount of current is available to drive other elements. The input current required to drive the basic gate is referred to as a standard load and the input current requirements and output capabilities of all other elements, called loading factors and fan-out respectively, are normalized to this. The input loading factor of the standard NOR gate is thus one and since the MC817P gate has a fan-out of 4, it can drive the equivalent of 4 standard gates. The loading rules are described in Motorola Application Note AN285, and the loading factors and fan-outs of the various units are indicated in the mwMRTL data sheet DS9055R1.

Since the fan-out of the MC817P NOR gate is four times its input loading factor, it can be used in the inverter configuration as an inverting buffer between a unit with low fan-out and up to 4 standard loads. The MC898P buffer with a much lower output impedence has a loading factor of 2 and a fan-out of 30 and can be used to drive a larger number of units.

The loading rules must be carefully followed, especially when driving flip flops since both the amplitude and rise and fall times of the output of a gate are affected if it is overloaded.

<u>Flip Flops</u> - The other basic unit of logic networks is the flip flop, also called a bistable multivibrator (multi) or binary. It is used as a binary divider or storage unit. The unit used here is the MC876P containing two JK flip flops. A description of various types of flip flops can be found in Motorola Application Note AN254 or Millman and Taub (1965) Chapter 10. What follows will be a black box description of the JK flip flop. The JK designation indicates that, unlike some types of flip flops, the output in this case is defined for any combination of inputs.

The JK flip flop symbol and truth table are shown below.



S = Set
T = Trigger
C = Clear
C_D= Direct Clear

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
0	0	$\overline{Q}_n$	Q_n
1	0	1	0
0	1	0	1
1	1	Q_n	$\overline{Q}_n$

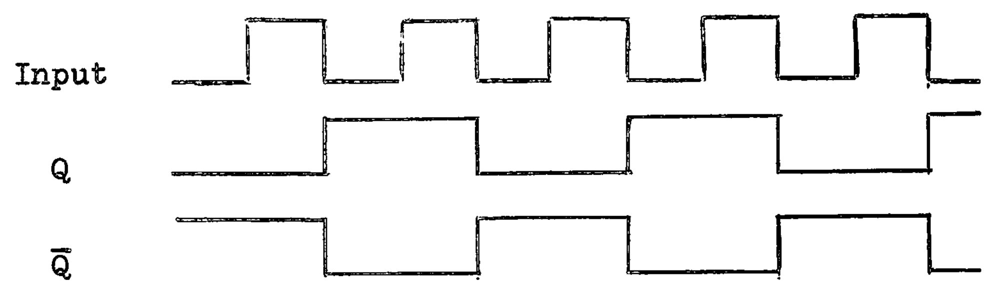
for $C_D = 1$ $Q = 0$, $\overline{Q} = 1$

t_n = before application of dynamic zero to T

t_{n+1} = after application of dynamic zero

C_D must be 0

The outputs Q and $\overline{Q}$ are always complements of each other, when one is in the 1 state the other is always 0. The two possible stable states are referred to as Set when Q is 1 and $\overline{Q}$ is 0, or Clear when Q is 0 and $\overline{Q}$ is 1. The MC876P can be forced into the Clear state by applying a positive level (1) to the C_D input. In the normal operating mode, with C_D at ground, any changes in the output state occur on applying a dynamic zero, or negative going pulse, to the trigger input T. Whether or not the output level changes depends on the state of the S and C inputs. In the simplest case, called the trigger mode, with both S and C at ground, the output changes state (flips or flops) with each dynamic zero at the trigger input. The flip flop thus goes through one half cycle for each cycle of the input and division by two has been accomplished.



The Set (S) and Clear (C) inputs can be used to force the output into a specified state, or inhibit it from changing state, on the following input trigger. If the output is in the Clear state (Q = 0, $\overline{Q}$ = 1) and the Clear input (C) is then made positive (1), the output will remain in the Clear state even on applying a dynamic zero to the input, T. Note that, unlike the direct Clear input (C_D)

which forces the flip flop into the Clear state as soon as it is applied, the S and C inputs only dictate what the output will be after the next input trigger is applied.

APPENDIX II

DIVISION NETWORKS

Frequency division in the clock requires four different division ratios. The flip flop alone is used for division by 2 as described in Appendix I. The various feedback networks necessary for division by 6, 10, and 24 are the subject of this Appendix.

Format - All division is performed by using an 8421 Binary Coded Decimal (BCD) format. In a BCD system each decimal digit is coded separately. Thus the number 681 would be represented by a code for 6, a code for 8 and a code for 1. The 8421 code uses the same representation as a simple binary code. The name 8421 is derived from the weights given each binary bit (i.e., each flip flop). The decimal equivalent of the 8421 code can be found by adding up the weights of those positions in which a 1 appears. The code for the numbers 1 to 9 is shown below. The order of the code has been reversed to 1248 to conform to the habit of reading from left to right.

	1	2	4	8	
0	0	0	0	0	0 + 0 + 0 + 0 = 0
1	1	0	0	0	1 + 0 + 0 + 0 = 1
2	0	1	0	0	0 + 2 + 0 + 0 = 2
3	1	1	0	0	1 + 2 + 0 + 0 = 3
4	0	0	1	0	0 + 0 + 4 + 0 = 4
5	1	0	1	0	1 + 0 + 4 + 0 = 5
6	0	1	1	0	0 + 2 + 4 + 0 = 6
7	1	1	1	0	1 + 2 + 4 + 0 = 7
8	0	0	0	1	0 + 0 + 0 + 8 = 8
9	1	0	0	1	1 + 0 + 0 + 8 = 9

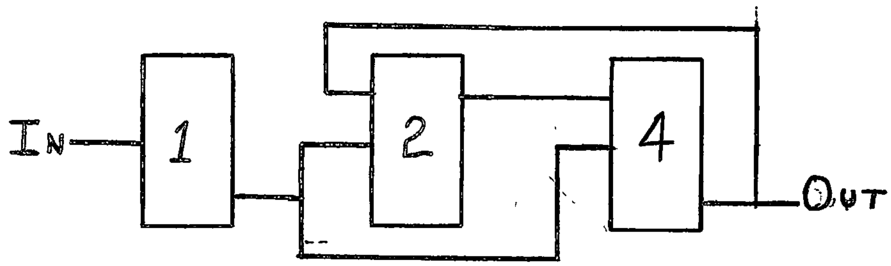
The use of flip flops in counting applications is obvious from the above table. If the columns 1248 are considered as the outputs of flip flops connected in series it can be seen that, reading down the table, each stage changes state when the preceding stage goes from 1 to 0 (a dynamic zero). This is the action of the flip flop as described in Appendix 1.

<u>Division</u> - Division in a logic system is essentially a counting procedure. If division by n is desired, the system counts n input pulses and gives one output pulse. A series of flip flops connected in series counts in a simple binary progression. To divide by a given number it is necessary to reset the chain of flip flops to zero when the required number is reached. The resetting is done with a feedback network using gates and the S and C inputs of the flip flops.

The networks for division by 6, 10 and 24 are described below. For a number of design reasons, including facility in decoding the output of the clock and compatibility with existing systems, the $\overline{Q}$ side of the output has been used as the active side of each flip flop. This leads to the situation in which all outputs are expressed in terms of the $\overline{Q}$ state of the flip flop. Thus the $\overline{Q}$ output of flip flop 39 in Figure 8 is referred to as "20 Hours" and the Q side is called "not 20 Hours" or $\overline{\text{20 Hours}}$, etc.

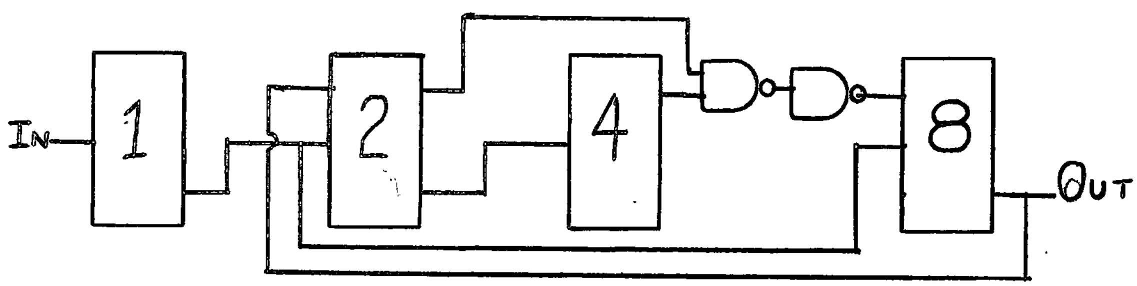
The following pages show the division ratios of interest. In each case the logic diagram is shown, along with the table of the $\overline{Q}$ state during the count. It is to be remembered that in all cases the Q state is simply the inverse of the $\overline{Q}$ state.

Also shown are the state of the S and C inputs that are used. The division scheme can be followed in each case by observing where the trigger input to each flip flop is connected and taking into account the state of the S and C inputs. In all cases the flip flops used are the MC876P and the gates and inverters are the 817P. Note that all inputs, not otherwise shown, are grounded.



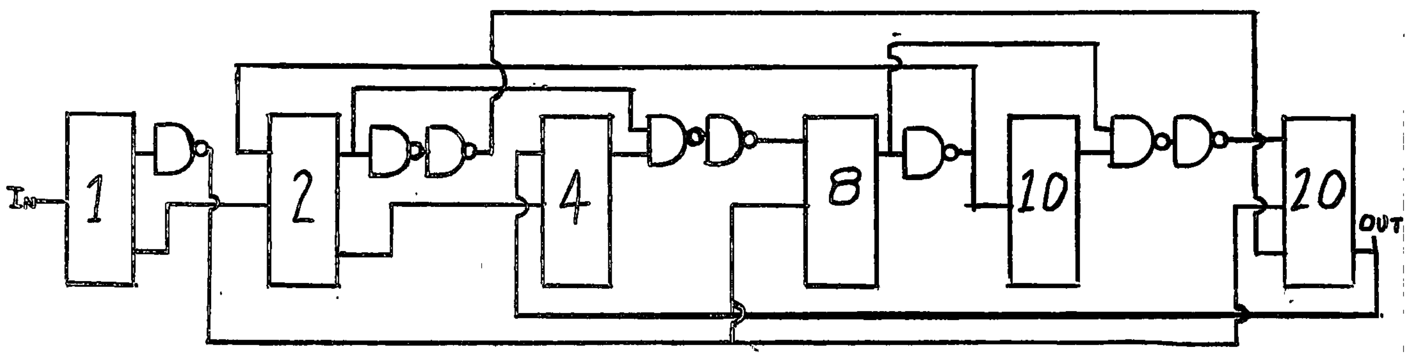
		$\bar{Q}$			
	1	2	4	$S_2=\bar{Q}_4$	$S_4=Q_2$
0	0	0	0	0	1
1	1	0	0	0	1
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	1	1
5	1	0	1	1	1
0	0	0	0	0	1

Table 4. Divide by 6



		$\bar{Q}$				
	1	2	4	8	$S_2=\bar{Q}_8$	$S_8=Q_2+Q_4$
0	0	0	0	0	0	1
1	1	0	0	0	0	1
2	0	1	0	0	0	1
3	1	1	0	0	0	1
4	0	0	1	0	0	1
5	1	0	1	0	0	1
6	0	1	1	0	0	0
7	1	1	1	0	0	0
8	0	0	0	1	1	1
9	1	0	0	1	1	1
0	0	0	0	0	0	1

Table 5. Divide by 10



	$\overline{Q}$										
	1	2	4	8	10	20	$S_2=\overline{Q}_8$	$S_4=\overline{Q}_{20}$	$S_8=Q_2+Q_4$	$S_{20}=Q_8+Q_{10}$	$C_{20}=Q_2$
0	0	0	0	0	0	0	0	0	1	1	1
1	1	0	0	0	0	0	0	0	1	1	1
2	0	1	0	0	0	0	0	0	1	1	0
3	1	1	0	0	0	0	0	0	1	1	0
4	0	0	1	0	0	0	0	0	1	1	1
5	1	0	1	0	0	0	0	0	1	1	1
6	0	1	1	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	1	0
8	0	0	0	1	0	0	1	0	1	1	1
9	1	0	0	1	0	0	1	0	1	1	1
10	0	0	0	0	1	0	0	0	1	1	1
11	1	0	0	0	1	0	0	0	1	1	1
12	0	1	0	0	1	0	0	0	1	1	0
13	1	1	0	0	1	0	0	0	1	1	0
14	0	0	1	0	1	0	0	0	1	1	1
15	1	0	1	0	1	0	0	0	1	1	1
16	0	1	1	0	1	0	0	0	0	1	0
17	1	1	1	0	1	0	0	0	0	1	0
18	0	0	0	1	1	0	1	0	1	0	1
19	1	0	0	1	1	0	1	0	1	0	1
20	0	0	0	0	0	1	0	1	1	1	1
21	1	0	0	0	0	1	0	1	1	1	1
22	0	1	0	0	0	1	0	1	1	1	0
23	1	1	0	0	0	1	0	1	1	1	0
0	0	0	0	0	0	0	0	0	1	1	1

Table 6. Divide by 24

APPENDIX 3

OPERATING PROCEDURE

This appendix contains an outline of setting the various components in the recording and playback systems, a list of pin and connector designations, battery types and field operation procedure. Note that the R_i's refer to the plugs (female) listed in Table 7 and the J_i's refer to the corresponding jacks (male).

Set up procedure

Record

Clock - see Figure 8 and Plate 5. The clock is set by comparison with an absolute time standard (WWV or CHU) or with a Master Clock system. The switches S_1 S_2 S_3 are all momentary contact micro-switches. S_1 disconnects the oscillator from the clock logic and "holds" the time. S_2 speeds up the counting rate by a factor of 2^5 and S_3 speeds it up by 2^{12}. S_2 thus cycles the clock through 2 hours in approximately 1 minute, and S_3 cycles it through 1 hour in approximately 1 second.

The clock is set by first attaching the readout to the clock output, R_1. The clock should first be checked by cycling it through one day by depressing S_3. S_3 is released when approaching the correct time and S_2 depressed until the minute ahead of absolute time is reached. S_1 is then depressed and held until the minute is reached.

As soon as it is set the clock should be calibrated by comparison with an absolute time. This can be done using a two channel chart recorder, one for the clock output (time check output R_{14}), and one for the absolute time standard.

Amplifier and Modulator - see Figures 2 and 4 and Plate 7. The gain of the amplifiers is controlled by two variables. The maximum gain of the first stage can be set by changing resistors R_{21} and R_{22} as described in Section 2.32. The input attenuator level is then selected by the position used in the attenuator network. Fifty db of attenuation is available. At present the first stage is set for 40 db gain and the second for 30 db, so that gains of -10 to +40 db are available at the low level output and from +20 to +70 db at the high level output.

The pass band of the amplifier can also be varied by changing the capacitors described in Section 2.32.

The DC offset of the two amplifier stages is set by adjusting Rv_1 and Rv_2 for a frequency of 750 Hz at the tape driver jack J6. Channel 2 (R_2 pins 2 and 9) is for low gain and is adjusted by Rv_1. Channel 3 (R_2 pins 3 and 10) is the high gain and is adjusted by Rv_2. The offset required at the amplifier outputs (R_4 and R_5) is approximately -1 Volt.

Switching - see Figure 12, Plate 6 and Table 2. Both the interval between recordings and the length of each record can be set using pins P1 to P12. P1 is the "on time" input and P2 is the "off time" input. All of the BCD clock outputs from .8 minutes to 2 hours are available and each can be used for switching on or off. They are listed in Table 2. It is necessary only to insert a jumper between the appropriate on time pin and P1 and the off time pin and P2.

Playback

Signal Demodulator - see Figure 22 and Plate 8. Rv_3 is adjusted to give a one shot pulse width of .5 milliseconds. This pulse width can be monitored at the input to the filter or (if Vref is not present) at the input to the switch at point A in Figure 22.

Vref Demodulator - see Figure 19 and Plate 8. The resistor Rv_4 determines the value of the constant current charging the capacitor C_{192}. It is set by applying a 720 Hz sine wave (20 mV) to the input of the Vref pre amp (pin 1 of R9) or replaying the Fref channel of the tape. The value of Vref is then set to +5 Volts (pin 1 of R_{10}).

Time Demodulator - see Figure 16 and Plate 8. The DC offset of the timing pulses is set by adjusting Rv_5. The pulses can be monitored at pin 4 of R_{10}.

Field Operation

The set up for field operation is shown in Plate 1.

The following is a step by step outline of the operation procedure.

1. Set the switching and gain as described earlier in this appendix.
2. Assemble the units as shown in Plate 1, changing any

batteries necessary. The battery lives are listed in Table 8.

3. Plug the clock readout into the clock output R_1.
4. Check the switching times by applying -6 Volts to R_{14}, turning the tape recorder on and slowly cycling the clock by using switches S_2 and S_3.
5. Remove the -6v from R_{14}, to keep the recorder from switching while setting the clock.
6. Set the clock as described in the last section.
7. Make a time calibration.
8. Check center frequency of the modulators by applying the test board to the input jack J_6, and adjust as described in the last section if necessary.
9. Insert the tape in the recorder and lock the reels in.
10. Bolt down all units.
11. Turn tape recorder to 15/16 ips and push start.
12. Attach -6 Volts to J_{14}.
13. Place in buoy, attaching input R_{13}.
14. To start recording cycle, connect together R_{14} and J_{14}.

<u>Playback</u>

1. Remove J_6.
2. Attach Uher Power Supply to the recorder through R_7.
3. Rewind the tape.
4. Attach Playback Panel input cable to R_6 and R_9.
5. Connect output pins of R_{10} to recorder and/or filters.
6. Find the desired record by replaying at 3 3/4 ips and

listening for the hours time code. Display time code on a Memo Scope to determine the hour of the recording. The input to any sensitive galvanometer should be removed or turned off when rewinding.

7. Make a record.

PLUG	PIN	TITLE	TYPE
R_1		Clock Output	24 pin Micro Ribbon
		see Table 1	
R_2		Switching & Tape Drivers	24 pin Micro Ribbon
	1	Channel 1 Hot (Fref)	
	2	Channel 2 " (Low Gain Signal)	
	3	Channel 3 " (High Gain Signal)	
	4	Channel 4 " (Time)	
	5	Ground	
	6	+4 Volts input	
	7	-6 Volts input	
	8	Channel 1 Cold	
	9	Channel 2 "	
	10	Channel 3 "	
	11	Channel 4 "	
	12	Recorder on Command	
	13	Time Check Output	
	14	Modulator 2 (high gain) input to tape driver	
	15	Modulator 1 (low gain) input to tape driver	
R_3		Signal Input	BNC Chassis Mount
R_4		Low Gain Amplifier Output	BNC Chassis Mount
R_5		High Gain Amplifier Output	BNC Chassis Mount
R_6		Tape Recorder Input	14 pin Micro Ribbon
	1	Channel 1 Hot	
	2	Channel 2 "	
	3	Channel 3 "	
	4	Channel 4 "	
	5	Ground	
	8	Channel 1 Cold	
	9	Channel 2 "	
	10	Channel 3 "	
	11	Channel 4 "	
	12	Recorder on Command	

Table 7. Connectors and Pin Numbers

PLUG	PIN	TITLE	TYPE
R_7		Uher Recorder Auxiliary Input (△)	
	3	+6 Volts (Ground)	
	6	-6 Volts	
R8		Portable Clock Readout	50 pin Micro Ribbon
	15	.1 minute	
	16	.2 minute	
	17	1 minute	
	18	2 minute (Note that all these	
	19	10 minute outputs are the same	
	20	20 minute as those in Table 1	
	21	1 hour and are actually the	
	22	2 hour $\overline{Q}$ output and should	
	23	10 hour be barred.)	
	24	20 hour	
	25	+4 Volts	
	40	.4 minutes	
	41	.8 minutes	
	42	4 minutes	
	43	8 minutes	
	44	40 minutes	
	46	4 hour	
	47	8 hour	
	50	Ground	
R_9 & R_{10}		Playback Panel Input and Output	14 pin Micro Ribbon
	1	Channel 1	
	2	Channel 2	
	3	Channel 3	
	4	Channel 4	
	8-11	Ground	
R_{11} & R_{12}		Clock Buffer Input and Output	50 pin Micro Ribbon
		same as R_8	
R_{13}		Signal Input	Microphone Plug
	1	Signal	
	2	Ground	
R_{14}		Tape Recorder Power and Time	Belling Lee (Female)
	A	Time Check Output	
	B	+6 Volts (Ground)	
	C	-6 Volts	

TABLE 7 CONT'D. CONNECTORS & PIN NUMBERS

PLUG	PIN	TITLE	
TS_1			Terminal Strip
	1	+4 V	
	2	Ground	
	3	-6 Volts	
	4	Time Check Output	

TABLE 7 CONT'D. CONNECTORS & PIN NUMBERS

BATTERY	TITLE	CAPACITY	VOLTAGE	DRAIN	LIFE (hrs)	LIFE (days)
B_1	Clock Osc.	1000 mAHr	+4V	6.5 mA	155	6.5
B_2	Clock Logic	75 AHr	-4V	300 mA	250	10.5
B_3 to B_6	Amplifiers and Modulators	350 mAHr	-1.4V	250 µA	1400	58
			+1.4V	500 µA	700	29
B_7	Tape Recorder	110 AHr	-6V	350 mA	Depends on recording schedule (250 hrs of active recording)	

Table 8. Battery Life

RESISTOR	LOCATION	VALUE
Rv_1	Low Gain Amplifier Offset	100 K
Rv_2	High Gain Amplifier Offset	100 K
Rv_3	Signal Demodulator	10 K
Rv_4	Vref Demodulator	500 ohms
Rv_5	Time Demodulator	10 K

Table 9. Variable Resistors

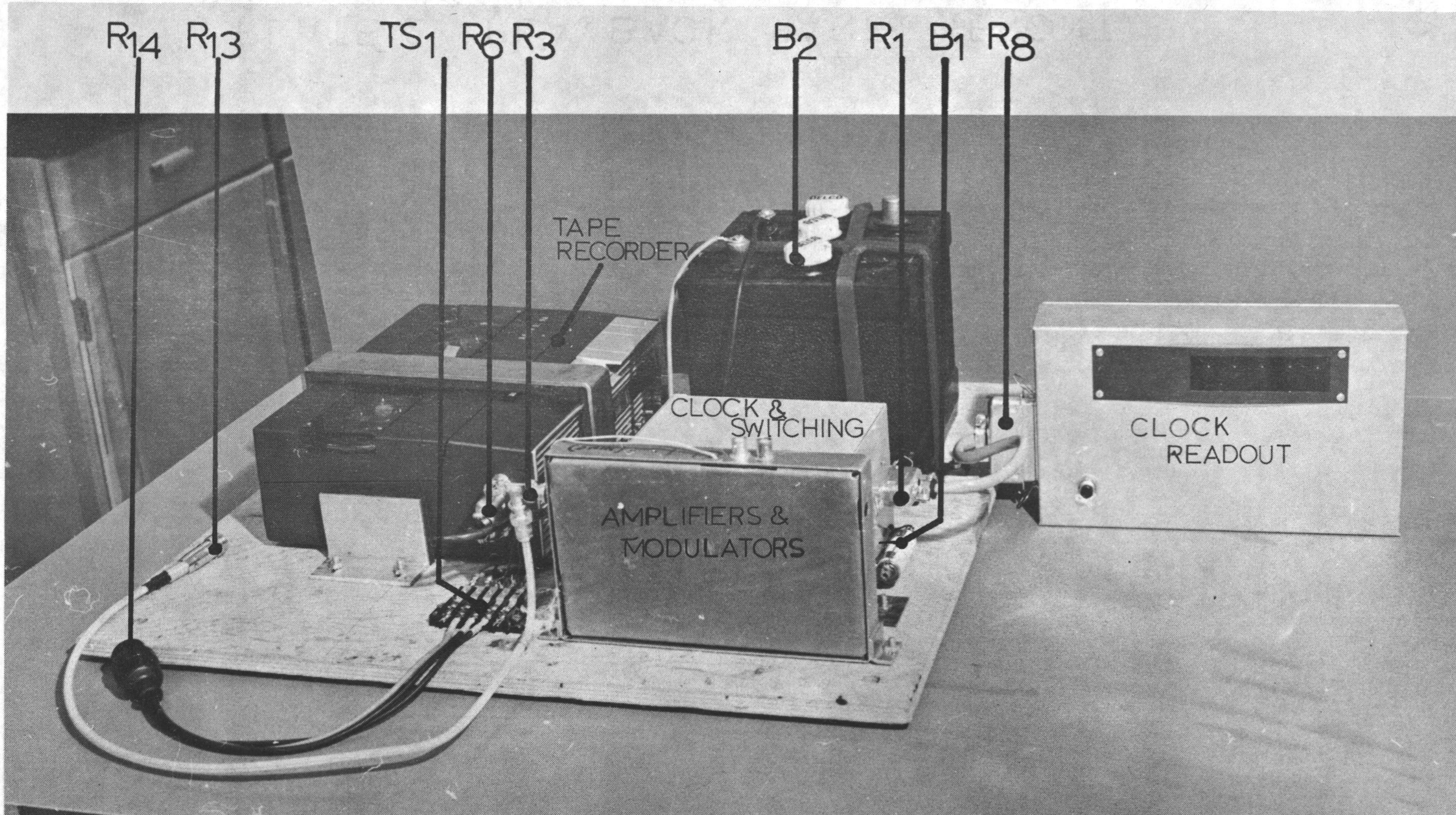


PLATE 1 RECORD SYSTEM

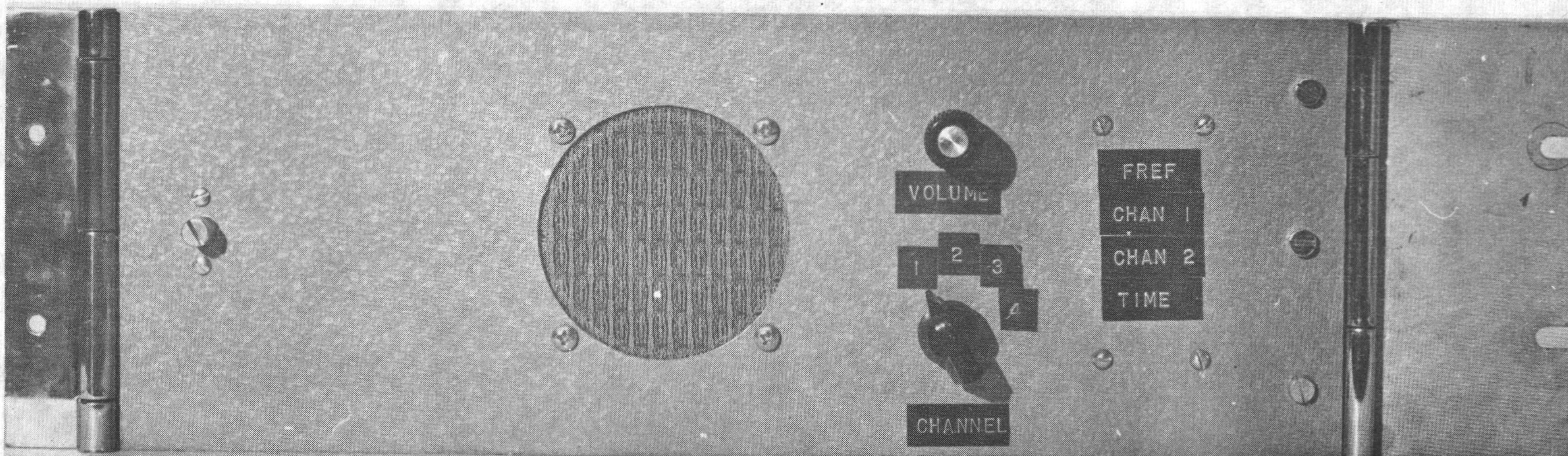


PLATE 2 PLAYBACK PANEL (FRONT)

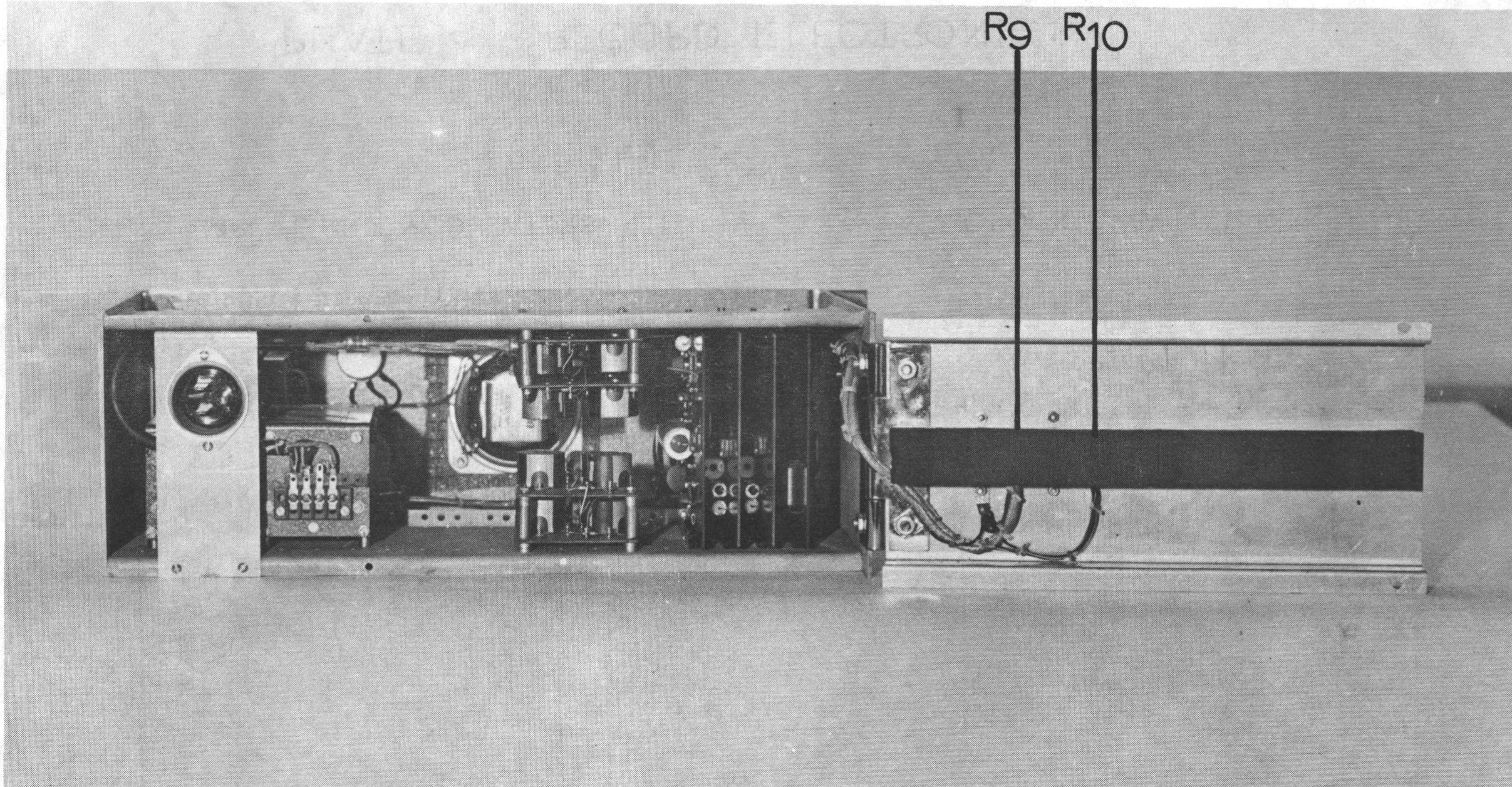
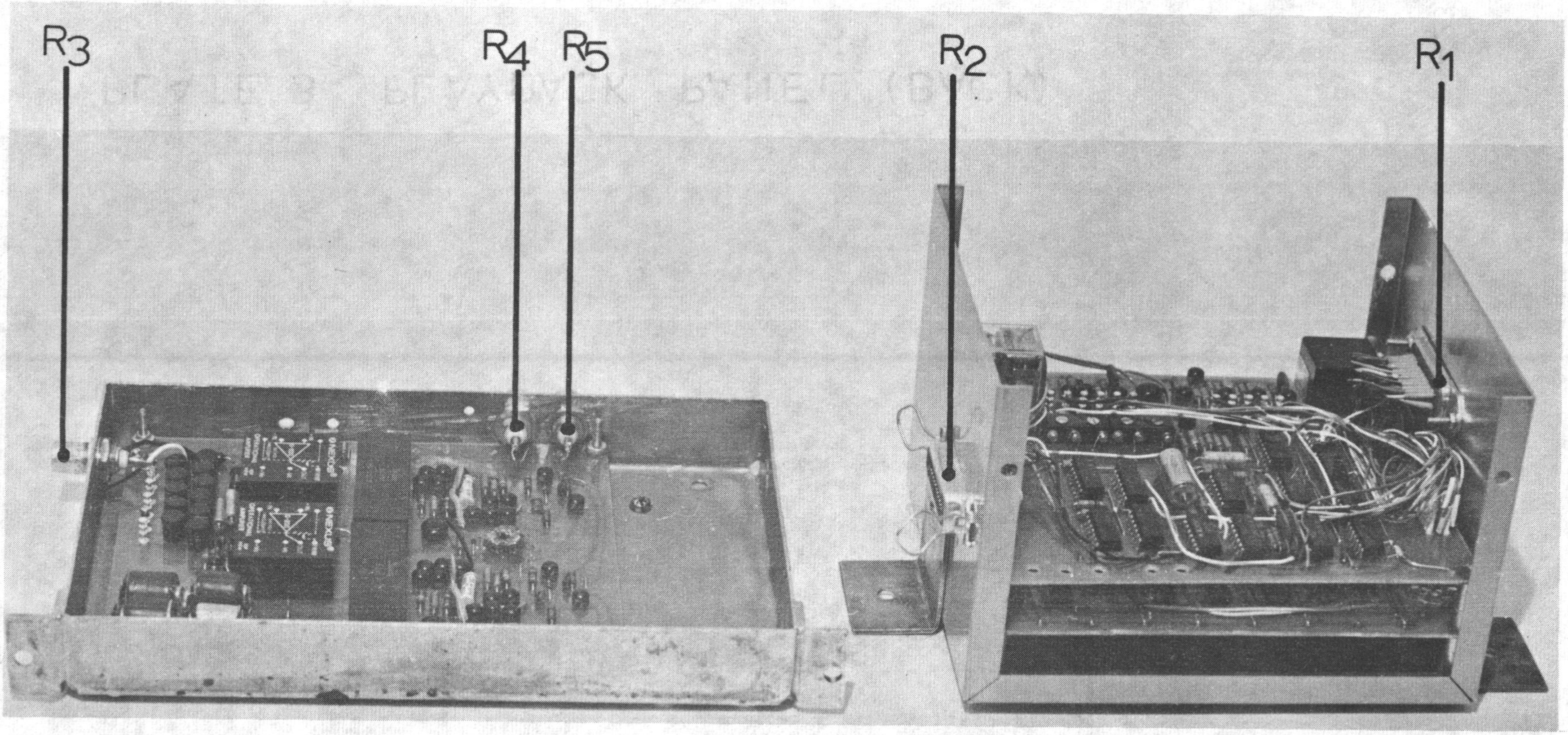


PLATE 3 PLAYBACK PANEL (BACK)



AMPLIFIERS & MODULATORS

CLOCK & SWITCHING

PLATE 4 RECORD ELECTRONICS

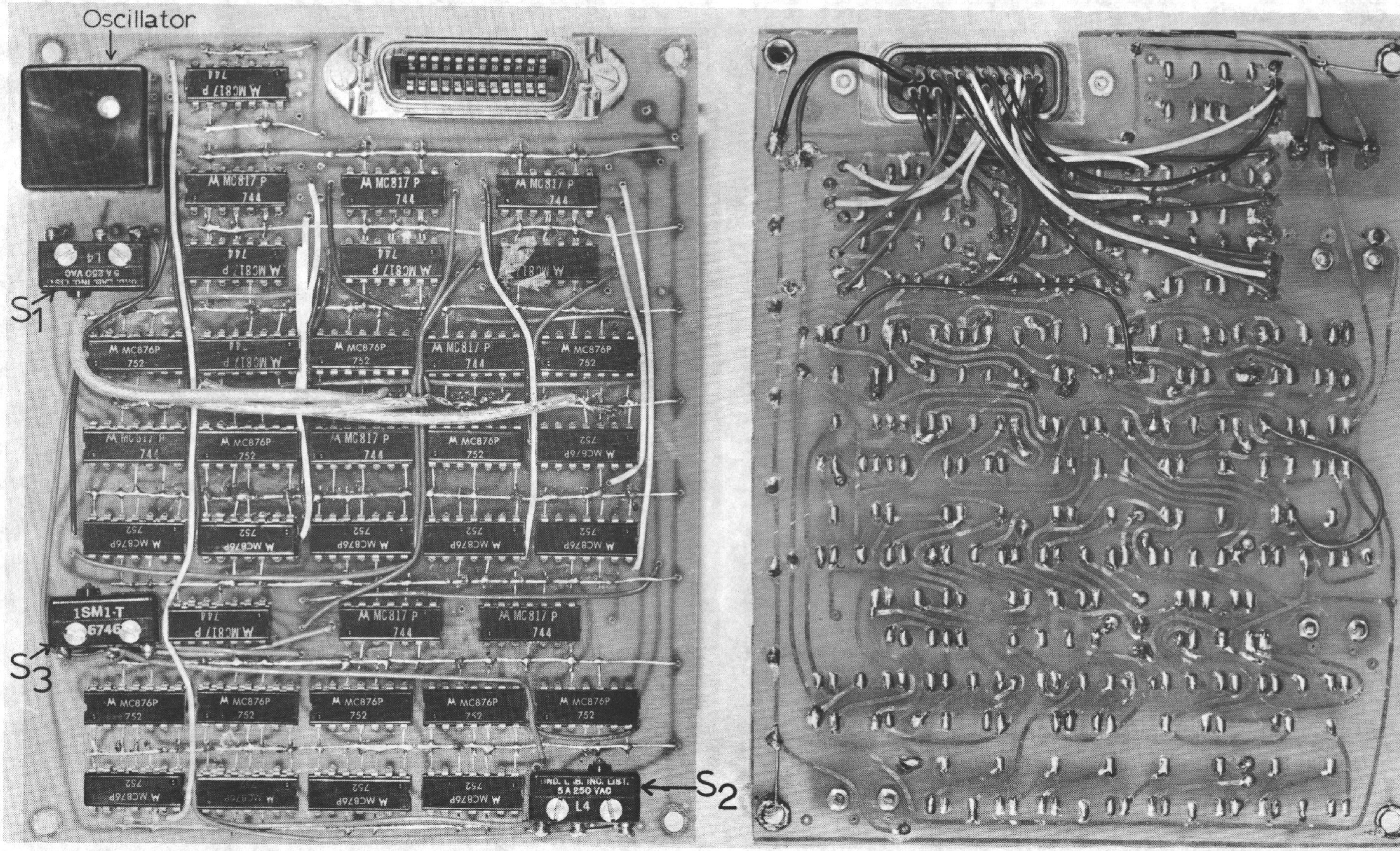


PLATE 5 THE CLOCK

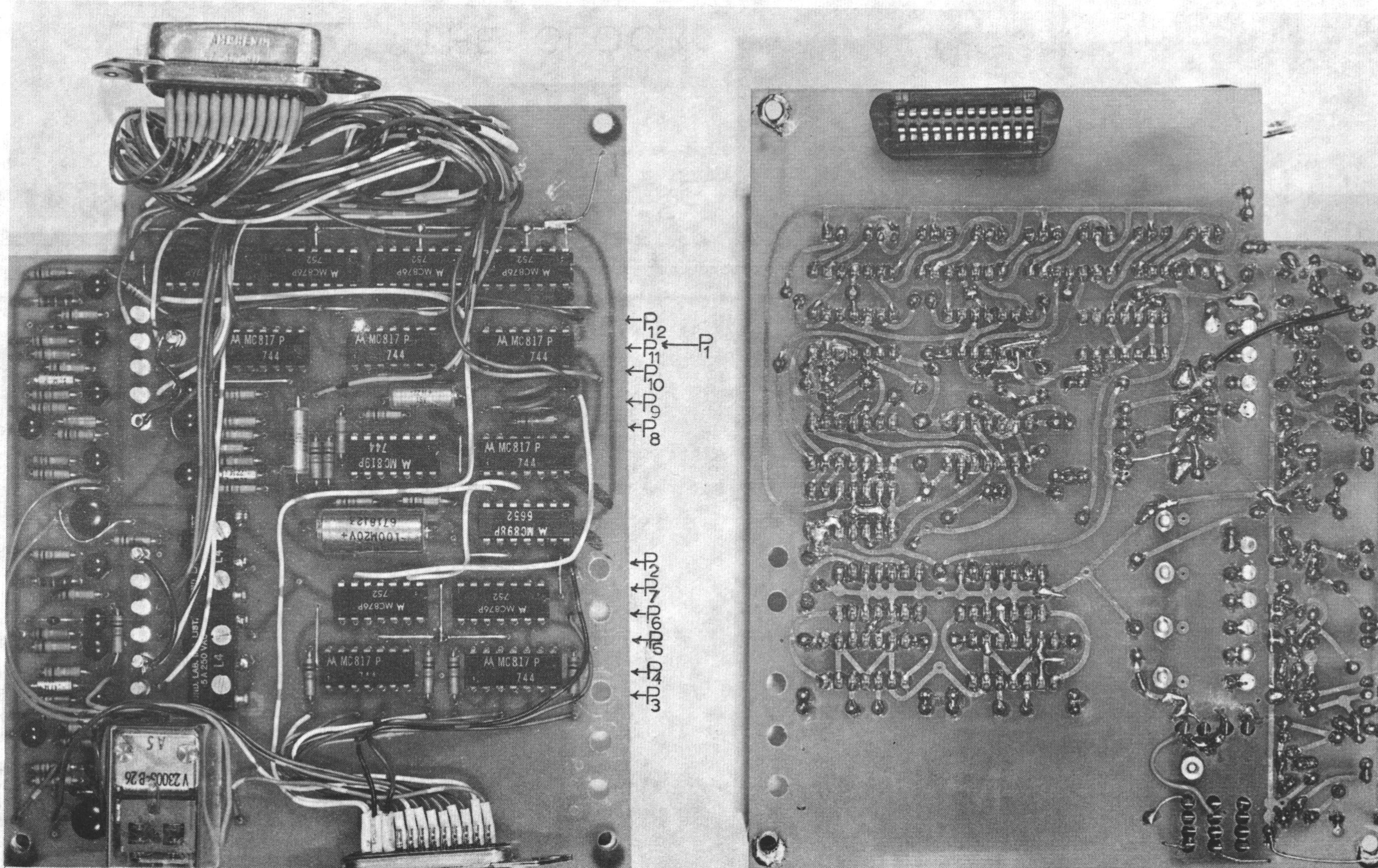


PLATE 6 TIMING and SWITCHING

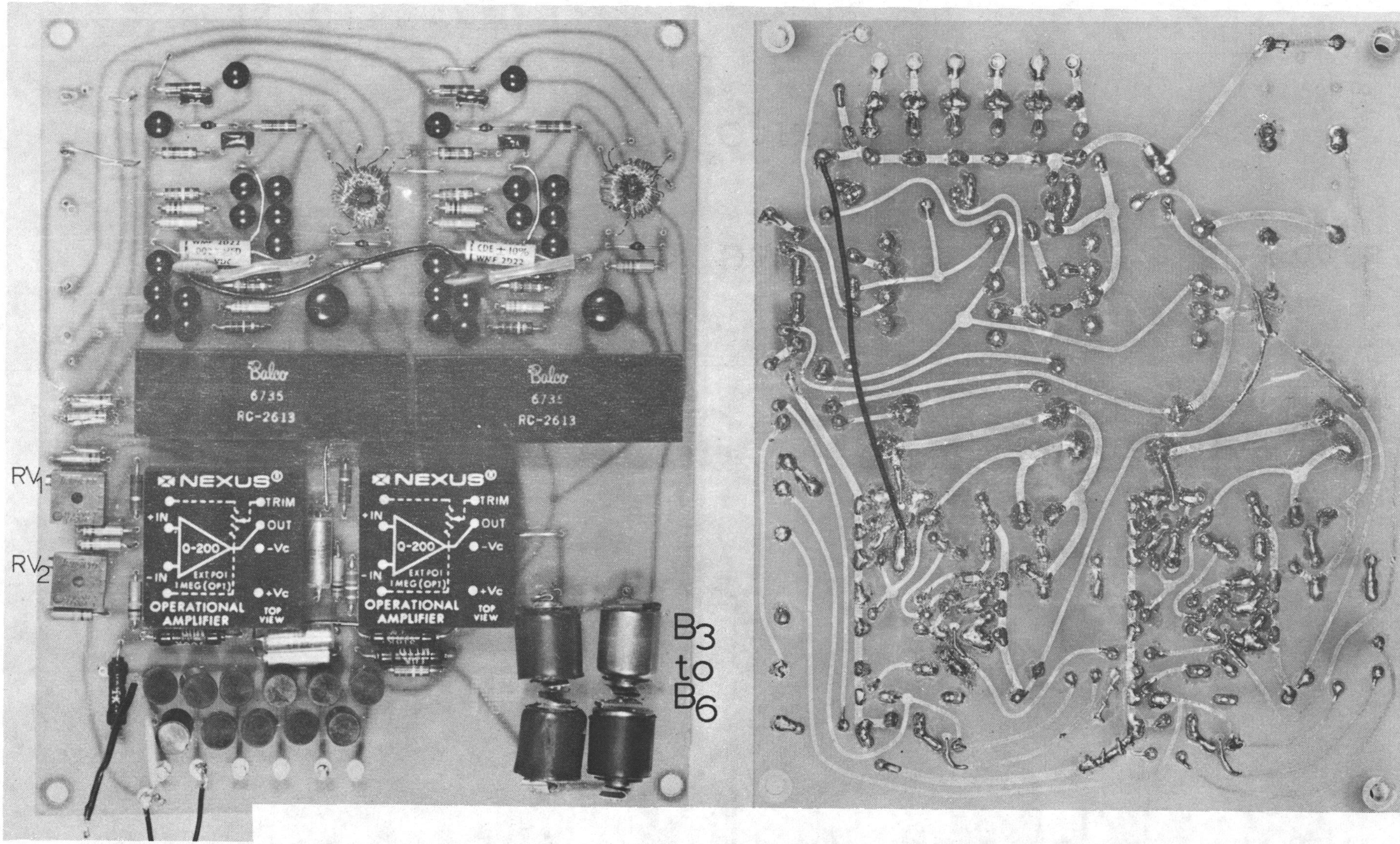
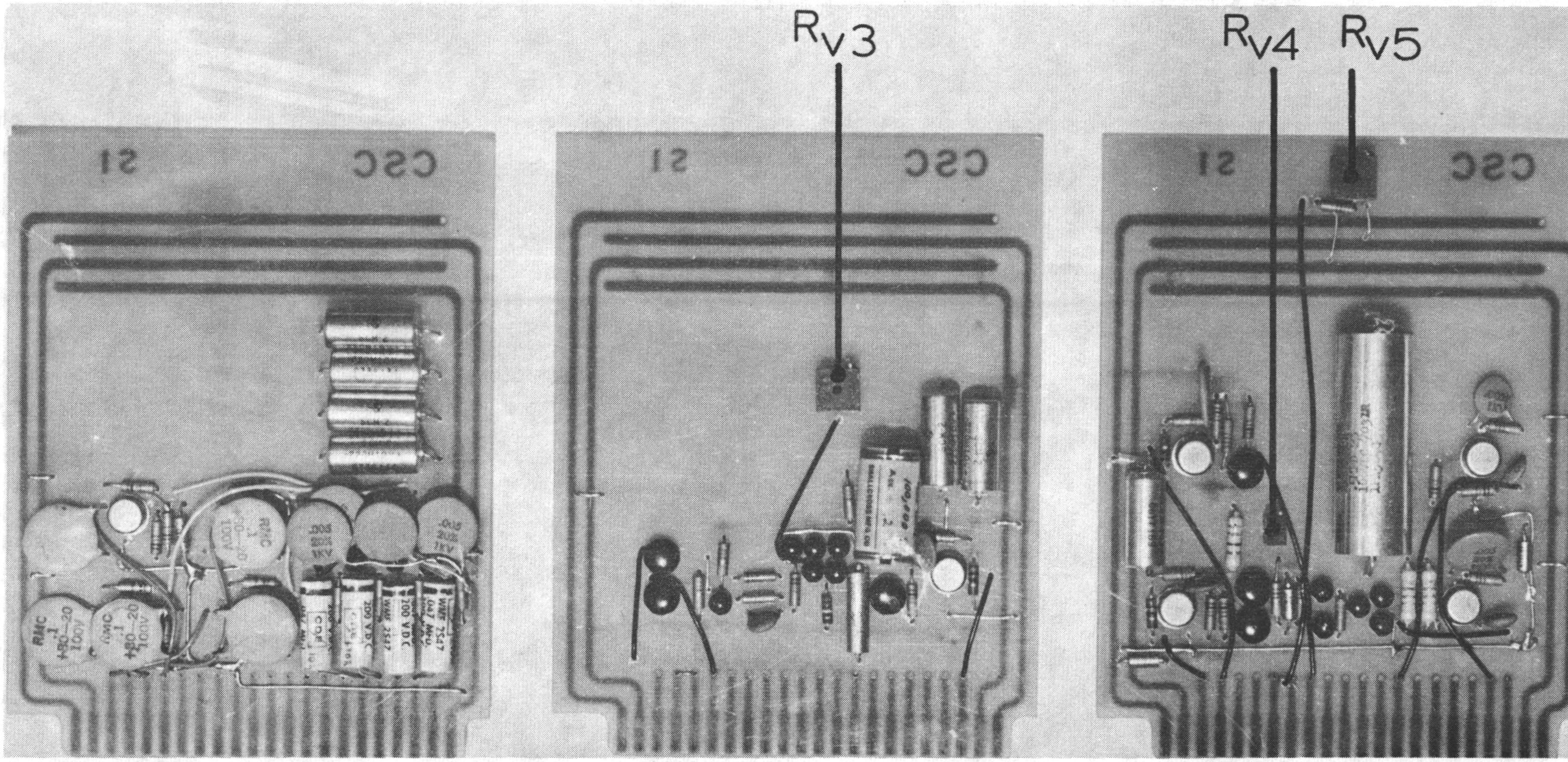


PLATE 7 AMPLIFIERS and MODULATORS



PreAmps Signal Demod Vref & Time Demods

PLATE 8 PLAYBACK CARDS

APPENDIX 4

COMPONENTS

Listed below are the semiconductors and main non-standard electrical components used in the recording and playback systems.

1 TRANSISTORS

2N3441	RCA	NPN Silicon Power Transistor
2N3565	Fairchild	NPN Silicon High Gain
2N3643	"	NPN Silicon High Current Switch
2N3644	"	PNP " " " "
2N3646	"	NPN " " Speed Saturated Switch
2N4122	"	PNP " " " Switch & RF Amplifier
2N4250	"	PNP " Low Level, Low Noise Amplifier
2N4917	"	" " High Speed Switch & RF Amplifier

2 DIODES

FDM6015	Fairchild	Silicon Fast switching, low capacitance

3 INTEGRATED CIRCUITS

μA702C(712)	Fairchild	High Gain, Wideband DC Amplifier
μA709C	"	High Performance Operational Amplifier
μA710C	"	High Speed Differential Comparator
CμL9960	"	Decimal Decoder/Driver
MC817P	Motorola	Quad 2-input RTL Gate

MC819P	Motorola	Dual 4-input RTL Gate
MC876P	"	Dual J.K. Flip Flop
MC898P	"	Dual 2-input Buffer

4 OPERATIONAL AMPLIFIER

Q-200	Nexus	Micropower Operational Amplifier

5 CONNECTORS

14, 24 and 50 pin   Amphenol 57 Series Micro Ribbon Miniature Cable and Chassis Connectors

6 RESISTORS & CAPACITORS

R.C. Network (Figure 4, R_{41} & C_{41})

Balco type RC2613   RC = .5msec ±.2% ±30ppm/°C

Capacitor (Figure 19, C_{191})

Component Research   1PA504G .5µf ±2%

Capacitor (Figure 22, C_{221})

Component Research   1PA502G .005µf ±2%

Resistor (Figure 22, R_{221})

Shalcross Bx193 Wire wound 100K ± .2%

Resistors (Figure 2 Attenuation Network)

Shalcross PC8E1A 131.6K, 192.5K and 284.6K ±.05%

7 READOUT TUBES

Burroughs Nixie Tubes B4032 (7977) Long Life

8 RELAY

Siemens Halske Bistable Magnetic Latching Relay

type U23003-B26-A5

9 CRYSTAL OSCILLATOR

Gibbs Manufacturing and Research	Model 562 TCXO Plastipac Series 184.32KHz

10 PULSE TRANSFORMER CORE

Indiana General	Ferramic Torroid Type H F625, CF102

11 TAPE RECORDER

Uher	Report 4000L	4 speed, ¼ inch tape, 5 inch reels

12 TAPE HEADS

Nortronics	5603	4 channel, Hyperbolic Metal Face, Laminated Core

13 MAGNETIC TAPE

Ampex	641	1 mil. Professional Audio Series
	746	1 mil. Instrumentation Type

14 POWER SUPPLY (Playback)

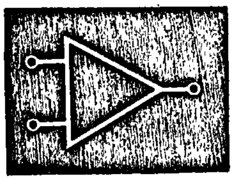
Farnell	Type MSU DC Power Supply

NEXUS
A TELEDYNE COMPANY

PB-142-9/67

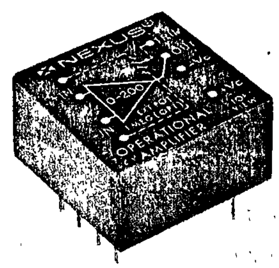
Q-200

MICROPOWER OPERATIONAL AMPLIFIER



SPECIAL FEATURES

- UNIVERSAL SUPPLY CAPABILITY - ±2V to ±15V TYPICALLY
- 4MΩ MINIMUM DIFFERENTIAL INPUT IMPEDANCE
- LOW QUIESCENT CURRENT - TYPICALLY 50μA
- USABLE "DEMAND" OUTPUT UP TO 3mA
- 12μV/°C TYPICAL OFFSET VOLTAGE STABILITY



GENERAL DESCRIPTION

NEXUS® type Q-200 is a new high stability micropower operational amplifier designed for indefinite operation with virtually "no" battery drain. This module is constructed of silicon semiconductors and other selected components to insure reliable operation over the temperature range of -25°C to +85°C. The Q-200 offers the flexibility of proper operation under a wide variety of supply voltages - typically ±2V to ±15V - with a typical quiescent drain current of 50μA @ ±3.5V. At the same time, it has the capability of supplying, upon demand, an I_o of 3mA @ E_o= 1V (±3.5V supply). This unit is internally compensated for low initial offset voltage (typically ±0.3mV) so that the use of an external potentiometer is optional but not required.

PROTECTION

The input circuitry of this amplifier is fully protected against damage due to accidental connection of the input terminals across the power supply. The output circuitry is also fully protected against short term short circuits to ground and to either power supply terminal at 25°C.

APPLICATIONS

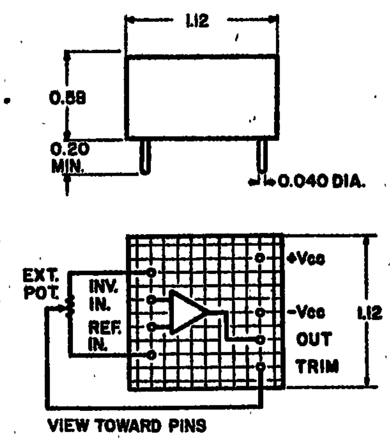
The Q-200 can be used in a wide variety of applications where power is at a premium. These include such fields as oceanography, aerospace, and medical instrumentation. For detailed applications assistance contact the NEXUS® Applications Engineering Department.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	-55°C to +100°C
Operating Temperature	-25°C to +85°C
Supply Voltage	±16 Volts

*Absolute Maximum Ratings correspond to the maximum stresses to which the amplifier can be subjected without permanent damage. Conformance to the electrical specifications under these conditions is not guaranteed.

PACKAGE OUTLINE AND BASE CONNECTION DIAGRAM



Case Size	Pin Dia. (In.)	Grid Spacing (In.)	Weight (gm.)	Volume (Cu.In)	Mating Socket
QB	.040	.1	30	.73	NSK-20

NEXUS® TYPE Q-200

Electrical specifications at 25°C and ±4.5 volt supply unless noted

CHARACTERISTICS	SYMBOL	TYPICAL	GUARANTEED	TEST CONDITIONS
RATED OUTPUT				
Usable Voltage Range	E_o	±3V	±1V (Min.)	R_{LL} = 1kΩ [1]
Maximum Current @ Full Output Voltage	I_o	±3mA	±1mA (Min.)	R_{LL} = 1kΩ [1]
Short Circuit to Ground	I_{ssg}	--	±12mA (Max.)	R_{LL} = short
COMMON MODE				
Rejection Ratio @ dc	CMRR	90dB	75dB (Min.)	E_{cm} = ±3V
Usable Input Voltage Range	E_{cm}	--	± 3.0V (Min.)	
OPEN LOOP GAIN	A_o	40,000	20,000 (Min.)	R_{LL} = 1kΩ [1]
FREQUENCY RESPONSE				
Small Signal Unity Gain Inverter	f_t	170kHz	150kHz (Min.)	R_i = 10kΩ; R_f = 10kΩ
Maximum Frequency for Full Output	f_p	1.5kHz	1kHz (Min.)	R_i = 10kΩ; R_f = 10kΩ; R_{LL} =1kΩ [1]
Slewing Rate	SR	9V/ms	3.0V/ms (Min.)	R_i = 10kΩ; R_f = 10kΩ; R_{LL} =1kΩ [1]
Max. Capacitive Loading w/out Causing Instability	C_L	1500pF	1200pF (Min.)	R_i = 10kΩ; R_f = 10kΩ
Gain Margin	--	--	6dB (Min.)	R_i = 10kΩ; R_f = 10kΩ
Phase Margin	--	--	30° (Min.)	R_i = 10kΩ; R_f = 10kΩ
RECOVERY TIME FROM OVERDRIVE	τ_{OL}	1.0ms	1.2ms (Max.)	R_i = 10kΩ; R_f = ∞ ; E_{in} = ±1.6V
SETTLING TIME (to 0.1% of final value)	τ_s	--	500µs (Max.)	R_i = 10kΩ; R_f = 10kΩ; E_{in} =±1V
INPUT VOLTAGE OFFSET				
Initial Value @ 25°C	E_{os}	0.3mV	1mV (Max.)	-- -- --
Temperature Coefficient	TCE_{os}	12µV/°C	20µV/°C (Max.)	-25°C to +85°C
vs. Power Supply	--	--	150µV/V (Max.)	±3.5V < V_{cc} <±5.5V
EXTERNAL OFFSET VOLTAGE TRIM POTENTIOMETER	R_{os}	1MΩ	--	Optional for Fine Trim [2]
INPUT BIAS CURRENT [3]				
Either Input @ 25°C	I_{bias}	12nA	25nA (Max.)	R_{test} = 1MΩ
Temperature Coefficient	TCI_{bias}	200pA/°C	400pA/°C (Max.)	-25°C to +85°C
vs. Power Supply	--	--	5nA/V (Max.)	±3.5V < V_{cc} <±5.5V
INPUT DIFFERENCE CURRENT				
Initial Value @ 25°C	I_{diff}	--	5nA (Max.)	R_{test} = 1MΩ
Temperature Coefficient	TCI_{diff}	--	100pA/°C (Max.)	-25°C to +85°C
vs. Power Supply	--	--	1nA/V (Max.)	±3.5V < V_{cc} <±5.5V
WIDEBAND INPUT NOISE VOLTAGE	e_n	--	2.8µVrms (Max.)	R_i = 100Ω; R_f = 10kΩ; BW=9kHz
INPUT IMPEDANCE				
Differential	Z_d	--	4MΩ (Min.)	Test Frequency = 10Hz
Common Mode	Z_{cm}	--	500MΩ (Min.)	Test Frequency = 10Hz
OUTPUT IMPEDANCE				
Open Loop	Z_o	--	5,000Ω (Max.)	Test Frequency = 10Hz
POWER SUPPLY				
Voltage (3-wire dc)	V_{cc}	--	±2.5V (Min.) to ±15V (Max.)	-- -- --
Current, Quiescent	I_{cc}	50µA	65µA (Max.)	-- -- --
Current, Full Output	I_{cc}	--	1.40mA (Min.)	R_{LL} = 1kΩ [1]

(1) R_{LL} is the parallel combination of feedback resistor R_f and external load resistance R_L.

(2) The Q-200 operational amplifier is internally trimmed; however, an optional external trim potentiometer may be used for fine trimming.

(3) Input Bias Current (I_{bias}) was formerly called Input Offset Current (I_{os}). The change in terminology is for the purpose of conforming to recent (but unofficial) conventional usage.

MC800P SERIES
MRTL INTEGRATED CIRCUITS

MAXIMUM RATINGS ($T_A = 25°C$)

Characteristic	Symbol	Rating	Unit
Logic Input Voltage		±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)		+12	Vdc
Power Dissipation	P_D	250	mW
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Milliwatt MRTL			MRTL			Unit
	0°C	+25°C	+75°C	0°C	+25°C	+75°C	
I_{A3}	0.420	0.430	0.395	1.8	1.8	1.71	mAdc min
I_{A4}	0.570	0.570	0.535	2.4	2.4	2.28	mAdc min
I_{A5}	—	—	—	3.0	3.0	2.85	mAdc min
I_{AB}	4.5	4.5	4.5	15.0	15.0	14.25	mAdc min
I_{CEX}	20	20	50	200	200	250	μAdc max
I_{in}	0.150	0.140	0.140	0.600	0.600	0.570	mAdc max
$2\ I_{in}$	0.300	0.280	0.280	1.2	1.2	1.1	mAdc max
I_L	100	100	100	—	—	—	μAdc max
V_{CE}	250	250	250	400	300	350	mVdc max
V_{out}	400	350	300	500	400	400	mVdc max

TEST CONDITIONS

V_{BOT}	1.8	1.8	1.8	1.8	1.8	1.8	Vdc
V_{CC}	3.6	3.6	3.6	3.6	3.6	3.6	Vdc
V_{in}	880	830	740	960	910	820	mVdc
V_{LL}	450	400	350	450	400	350	mVdc
V_{off}	500	460	400	570	500	450	mVdc
V_{on}	850	800	710	930	880	790	mVdc
V_R	—	—	—	640	640	750	Ohms
V_{RH}	4600	4600	5000	—	—	—	Ohms
V_{RL}	2700	2700	2800	—	—	—	Ohms

GENERAL RULES

1. The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
2. All unused inputs should be returned to ground.
3. V_{CC} is applied to Pin 11 with Pin 4 grounded.
4. Expander Rules:
   (1) The MC885P and MC886P MRTL expanders can be used to expand medium-power MRTL output nodes only.
   (2) Subtract 0.5 from the output loading factor of the MRTL expanded gate for each expander node that is connected.
   (3) The input loading factor of the MRTL expanded gate must be increased to 1.33.

DEFINITIONS

I_{A3}, I_{A4}, I_{A5} — Minimum available output current from a device with an output loading of 3, 4, or 5. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{in}.

I_{CEX} — Collector current of gate expander when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

$2\ I_{in}$ — Maximum input current drawn by one input of the MC898P or MC899P buffers with V_{in} applied. The other input is returned to V_{BOT}.

I_L — Leakage current of device when test voltage is applied. V_{CC} is the test voltage used on devices having all transistors in the "off" state. V_{LL} is the test voltage used on devices having one or more transistors in the "on" state (e.g. flip-flops).

V_{BOT} — A high-value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

V_{CE} — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high-level voltage applied to the input of a device.

V_{LL} — A low-value voltage applied to a device for testing I_L.

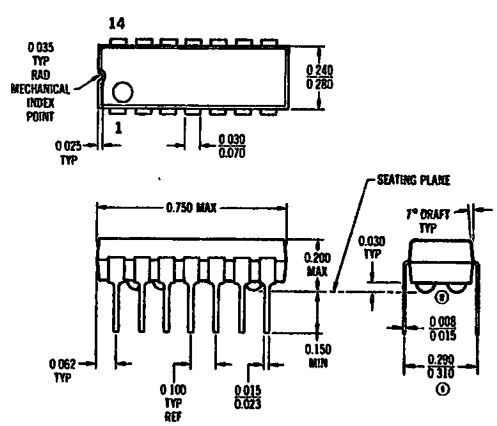
V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

OUTLINE DIMENSIONS



① This dimension is measured at the seating plane.
② 4 insulating stand-offs are provided.

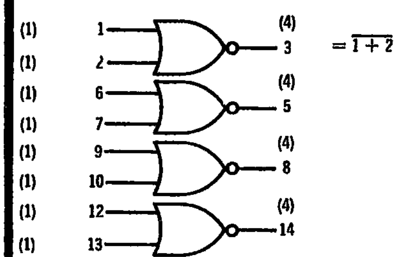
LOGIC DESCRIPTION

The logic diagrams shown describe the MC700P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability — fan-out — (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown on pages 2 and 3. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C with V_{CC} = 3.6 V ±10%.

All elements in the MC700P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

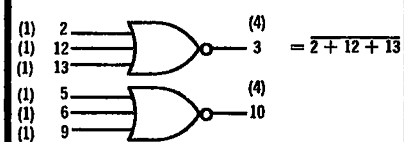
MC717P — QUAD 2-INPUT GATE



t_{pd} = 27 ns

P_D = 20 mW (Inputs High)
12 mW (Inputs Low)

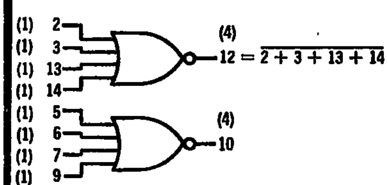
MC718P — DUAL 3-INPUT GATE



t_{pd} = 27 ns

P_D = 12 mW (Inputs High)
6 mW (Inputs Low)

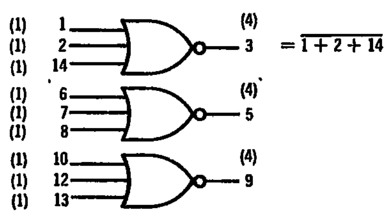
MC719P — DUAL 4-INPUT GATE



t_{pd} = 27 ns

P_D = 13 mW (Inputs High)
6 mW (Inputs Low)

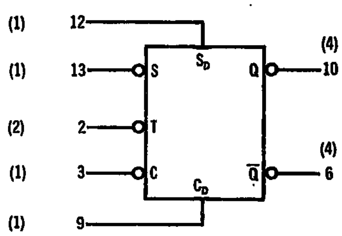
MC793P — TRIPLE 3-INPUT GATE



t_{pd} = 27 ns

P_D = 18 mW (Inputs High)
9 mW (Inputs Low)

MC722P — J-K FLIP-FLOP



f_{Tog} = 1 MHz

P_D = 35 mW (Only Clock Input High)
18 mW (Inputs Low)

DIRECT INPUT OPERATION(1)

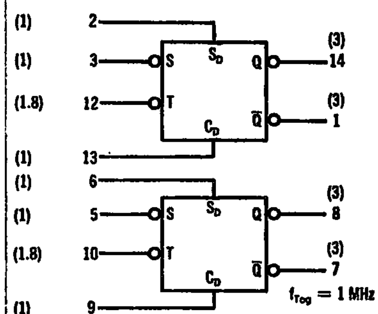
S_D	C_D	Q	$\bar{Q}$
0	0	(2)	(2)
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION(3)

t_n(4)		t_{n+1}(4)	
S	C	Q	$\bar{Q}$
1	1	Q_n(5)	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n(5)

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC778P — DUAL TYPE "D" FLIP-FLOP



f_{Tog} = 1 MHz

P_D = 40 mW (Direct Set, S_D, and Direct Clear, C_D, Low; all other inputs high)
35 mW (All Inputs Low)

DIRECT INPUT OPERATION(1)

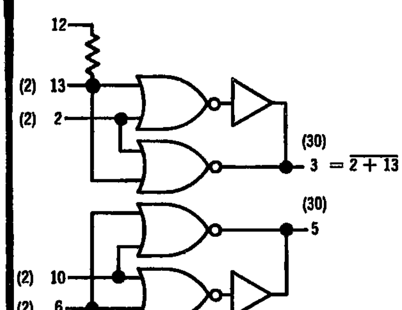
S_D	C_D	Q	$\bar{Q}$
0	0	(2)	(2)
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION(3)

t_n(4)	t_{n+1}(4)	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

MC798P — DUAL 2-INPUT BUFFER

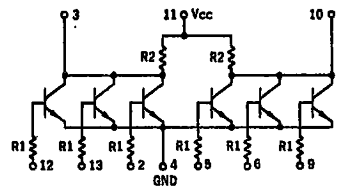


t_{pd} = 57 ns

P_D = 14 mW (Inputs High)
46 mW (Inputs Low)

CIRCUIT SCHEMATICS

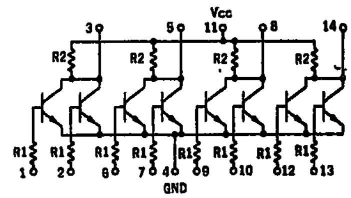
MC715P — DUAL 3-INPUT GATE



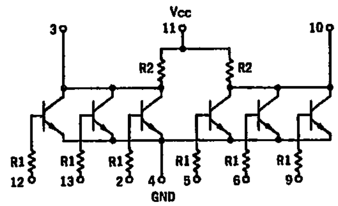
R1 = 450 Ω
R2 = 640 Ω

MC717P — QUAD 2-INPUT GATE

R1 = 1.5 kΩ
R2 = 3.6 kΩ



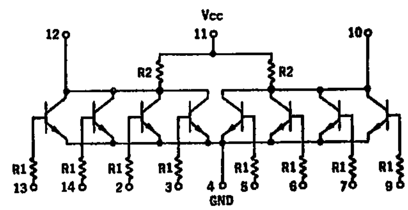
MC718P — DUAL 3-INPUT GATE



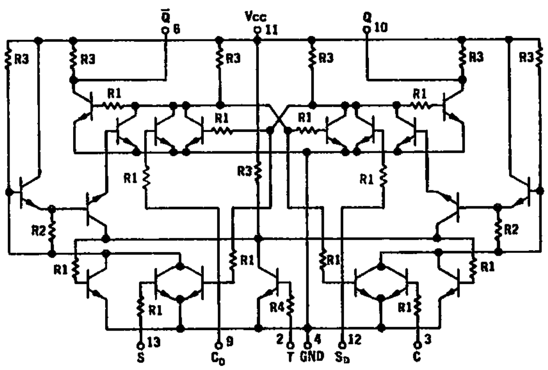
R1 = 1.5 kΩ
R2 = 3.6 kΩ

MC719P — DUAL 4-INPUT GATE

R1 = 1.5 kΩ
R2 = 3.6 kΩ

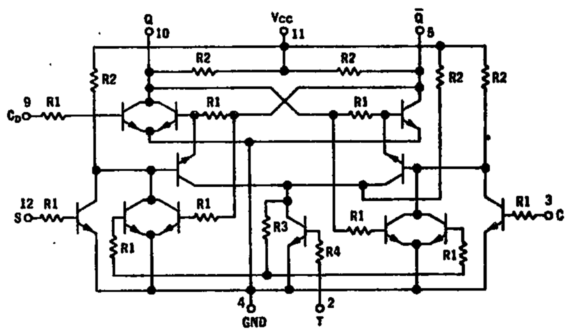


MC722P — J-K FLIP-FLOP



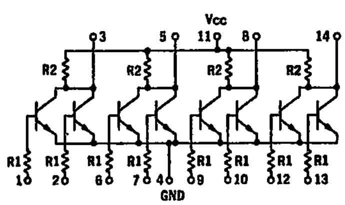
R1 = 1.5 kΩ
R2 = 2.0 kΩ
R3 = 3.6 kΩ
R4 = 750 Ω

MC723P — J-K FLIP-FLOP



R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

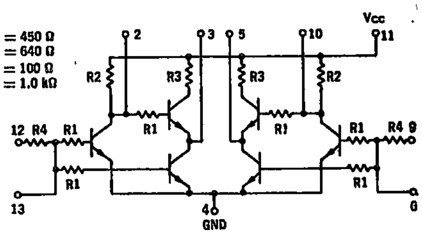
MC724P — QUAD 2-INPUT GATE



R1 = 450 Ω
R2 = 640 Ω

MC799P — DUAL BUFFER

R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω
R4 = 1.0 kΩ



RESISTOR VALUES ARE TYPICAL.

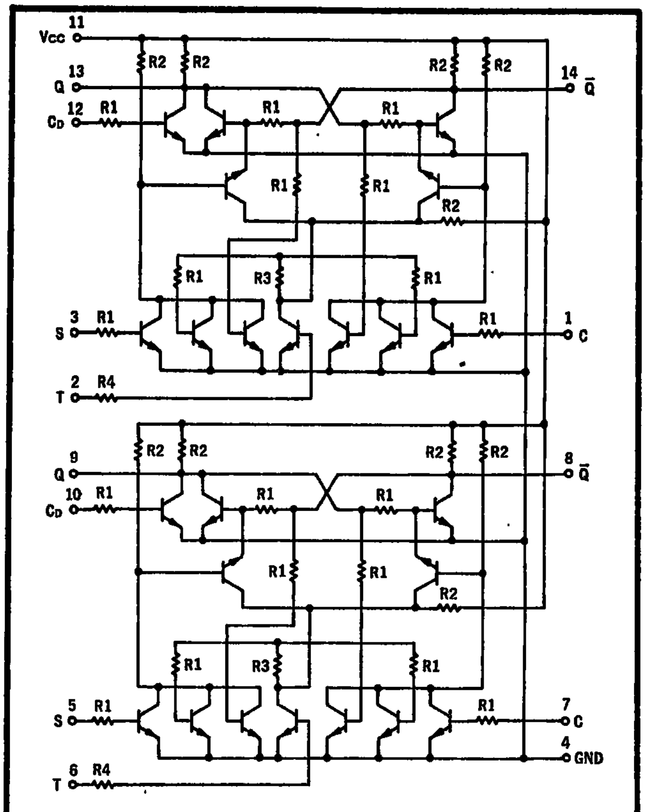
DUAL J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

MOTOROLA

MC776P · MC876P

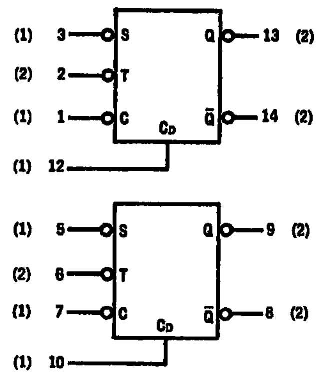
OCTOBER 1967



TYPICAL RESISTANCE VALUES

R1 = 1.5k R3 = 3.0k
R2 = 3.6k R4 = 750Ω

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{TOG} = 3 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (All Inputs Low)

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

CLOCKED INPUT OPERATION(1)

t_n (2)		t_{n+1} (2)	
S	C	Q	Q̄
1	1	Q_n (3)	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n (3)

(1) Direct input (C_D) must be low.

(2) The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

(3) Q_n is the state of the Q output in the time period t_n.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	µA I_D
MC876P	0°C	0.880	0.850	1.80	0.500	3.60	270
	+25°C	0.830	0.800	1.80	0.460	3.60	290
	+75°C	0.740	0.710	1.80	0.400	3.60	255
MC776P	+15°C	0.865	0.865	1.80	0.475	3.60	270
	+25°C	0.850	0.850	1.80	0.460	3.60	270
	+55°C	0.800	0.800	1.80	0.430	3.60	270

ELECTRICAL CHARACTERISTICS

TEST PROCEDURES ARE SHOWN FOR ONE FLIP-FLOP ONLY. THE OTHER FLIP-FLOP IS TESTED IN THE SAME MANNER.

Characteristic	Symbol	Pin Under Test	MC876P Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit	MC776P Test Limits +15°C Min	Max	+25°C Min	Max	+55°C Min	Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	I_D	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	µAdc	-	150	-	150	-	150	µAdc	1	-	13	-	11	-	4
	$2 I_{in}$	2	-	300	-	280	-	280	↓	-	300	-	300	-	300	↓	2	-	1, 3	-	↓	-	↓
	I_{in}	3	-	150	-	140	-	140	↓	-	150	-	.150	-	150	↓	3	-	14	-	↓	-	↓
	I_{in}	12	-	150	-	140	-	140	↓	-	150	-	150	-	150	↓	12	-	14	-	↓	-	↓
Output Current	I_{A2}	13	270	-	290	-	255	-	µAdc	270	-	270	-	270	-	µAdc	-	13	1	12	11	-	4, 14 §
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	-	↓
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12, 14	3	-	↓	-	↓
Output Voltage	V_{out}	13	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	↓	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	4, 13 §
		13*†	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	14	4, 12
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	3	↓	↓	↓
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	-	14 §
Saturation Voltage	$V_{CE(sat)}$	13	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	-	4, 13 §
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	12	↓	-	4, 14 §
Turn On Voltage	V_{on}	13*#	850	-	800	-	710	-	mVdc	865	-	850	-	800	-	mVdc	-	1, 3	-	-	11	13	4, 12
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	-	1	↓	↓	↓
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	-	1, 3	↓	↓	↓

* Clock Pulse to pin 2
† Pin 13 = LOW } Set by a momentary ground prior to the
# Pin 14 = LOW } application of the negative-going clock.

§ ground thru diode (cathode to ground).
Ground inputs of flip-flop not under test.
Other pins not listed are left open.